Waveform Generation

Lecture - 16

(29/04/2021)

B.Sc (Electronics)

TDC PART - III

Paper – 6

Unit – 8

by:

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➢ Transistor Bi-Stable Multivibrator Circuit Details (PART – 2)

⇨ The **basic typical Transistor Bi-stable Multivibrator** circuit diagram is **shown below in Figure (2).** The following circuit designed using **Two NPN Bipolar Junction Transistor (BJT)** namely **Q1 and Q2** along with **Four Resistors** such as **R1, R2, R3,** and **R4** and **Two Input Coupling Capacitor C1** and **C2.**

⇨ It consist **Two identical CE Amplifier Stages** with similar **Transistors Q1** and **Q2** along with **Load Resistors RL1** and **RL2** are **connected in feedback to one another.** It consists of **Two identical CE Amplifier Stages** with output of one fed to the input of the other. The feedback is coupled through **Feedback Resistors R2** and **R1.**

⇨ Here, **Collector Terminal of Transistor Q1** is coupled to **Transistor Q2** base through **Resistor R2 and Collector terminal of Transistor Q2** is coupled to **Transistor Q1** base through **Resistor R1.** It consists of **two similar NPN Transistors Q1** and **Q2** with **equal Collector Loads Resistor i.e. $R_{L1} = R_{L2}$.**

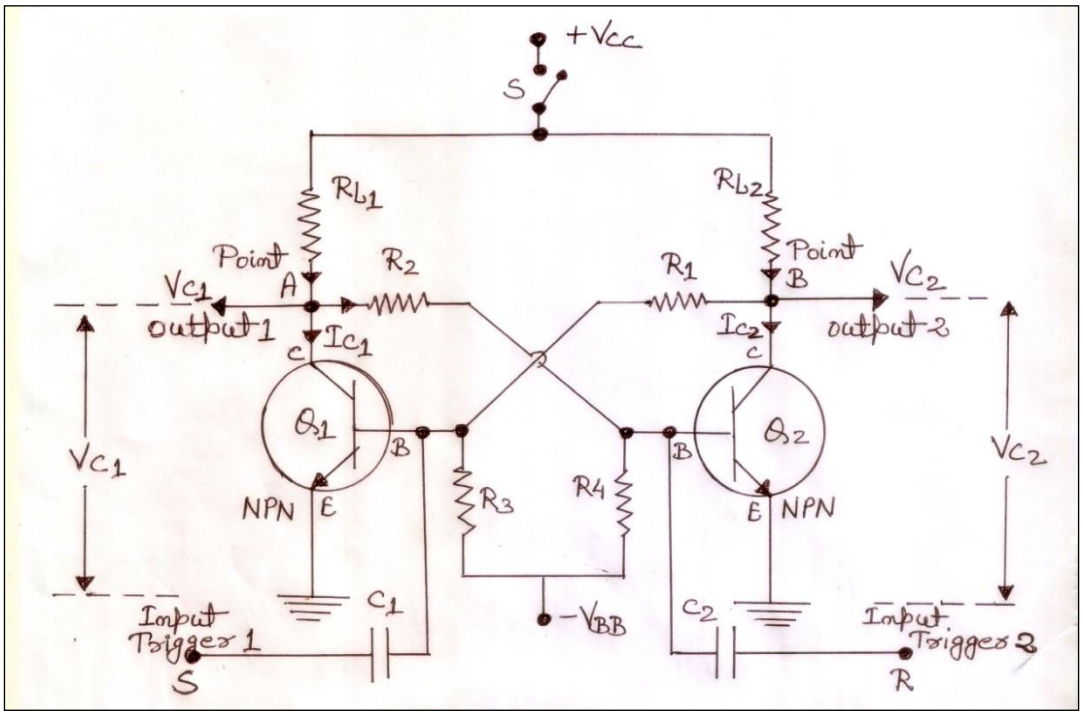

Fig (17) Shown a Basic Transistor Bistable Multivibrator (BMV) Circuit Diagram.

⇨ **Transistor Q1** and **Q2** connected with **Common Positive Supply Source $+V_{BB}$** through **Load Resistor R_{L1} and R_{L2}.** In the **BMV circuit diagram** the function of **Load resistors R_{L1}** and **R_{L2}** is to **limit collector current of both Transistors Q1** and **Q2.** The **Base Resistors R3 and R4** are joined to a **Common Negative Supply Source $-V_{BB}$.**

⇨ The **Transistor Q1** is given an **input trigger pulse** at the **Base Terminal** through the **Capacitor C1 and Transistor Q2** is given an **input trigger pulse** at the **Base Terminal** through the **Capacitor C2.**

⇨ The **output can be taken across collector terminal** of either **Transistor Q1 or Q2**. To **obtain output**, it can be taken from **Collector Terminal of NPN Transistor Q1 at Point A (output 1) or NPN Transistor Q2 at Point B (output 2).** The **output** can be taken across **Transistor Q1** is denoted as $\mathbf{V_{C1}}$ and **output** taken across **Transistor Q2** is denoted as $\mathbf{V_{C2}}$**.**

⇨ Detailed **of the Transistor Bi-Stable Multivibrator Circuit Operation** is discussed in next **Lecture – 17.**

to be continued .....

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