Silicon Controlled Rectifier (SCR)

Lecture – 8

TDC PART – I
Paper - II (Group - B)
Chapter - 5

by:

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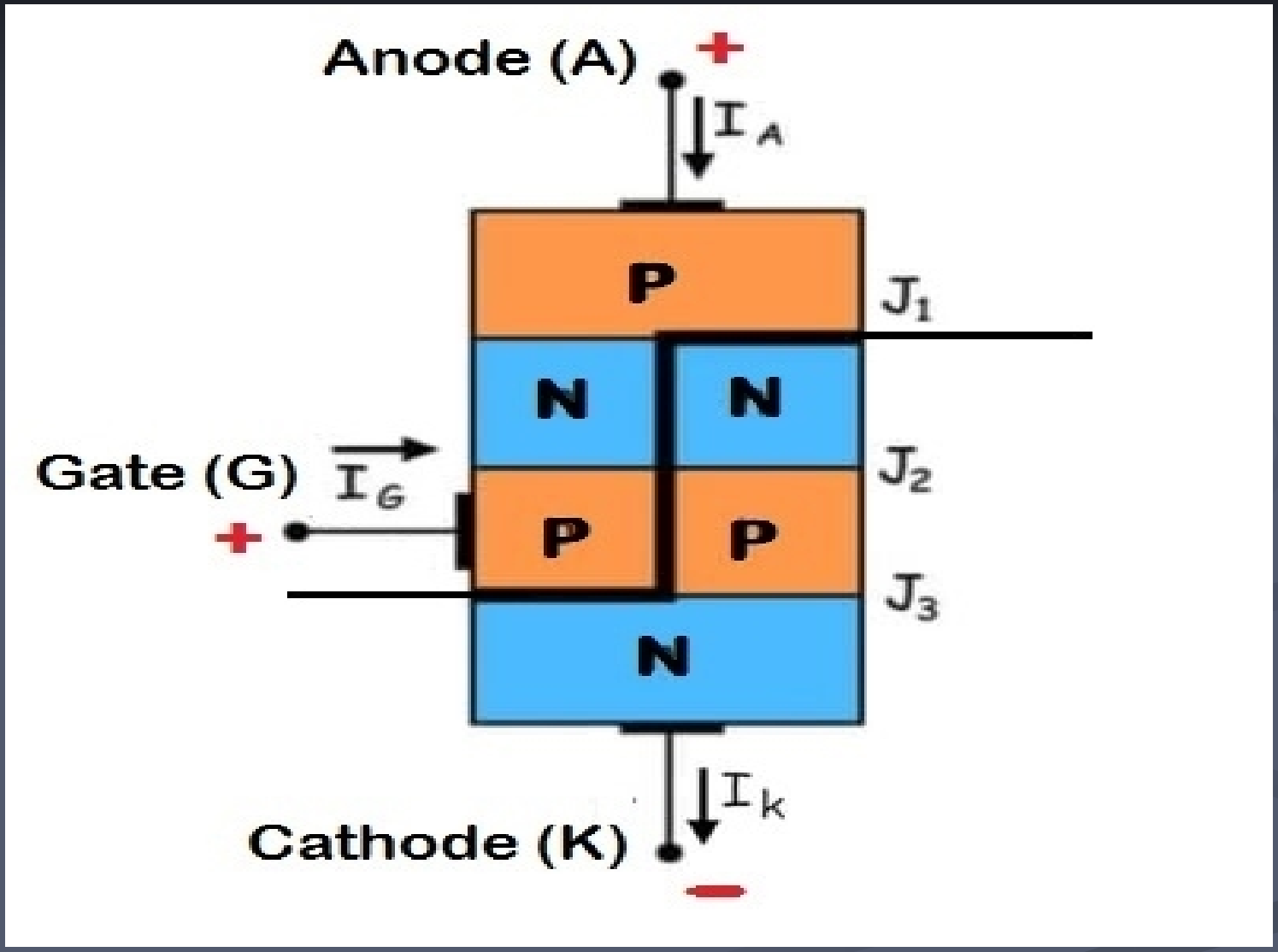
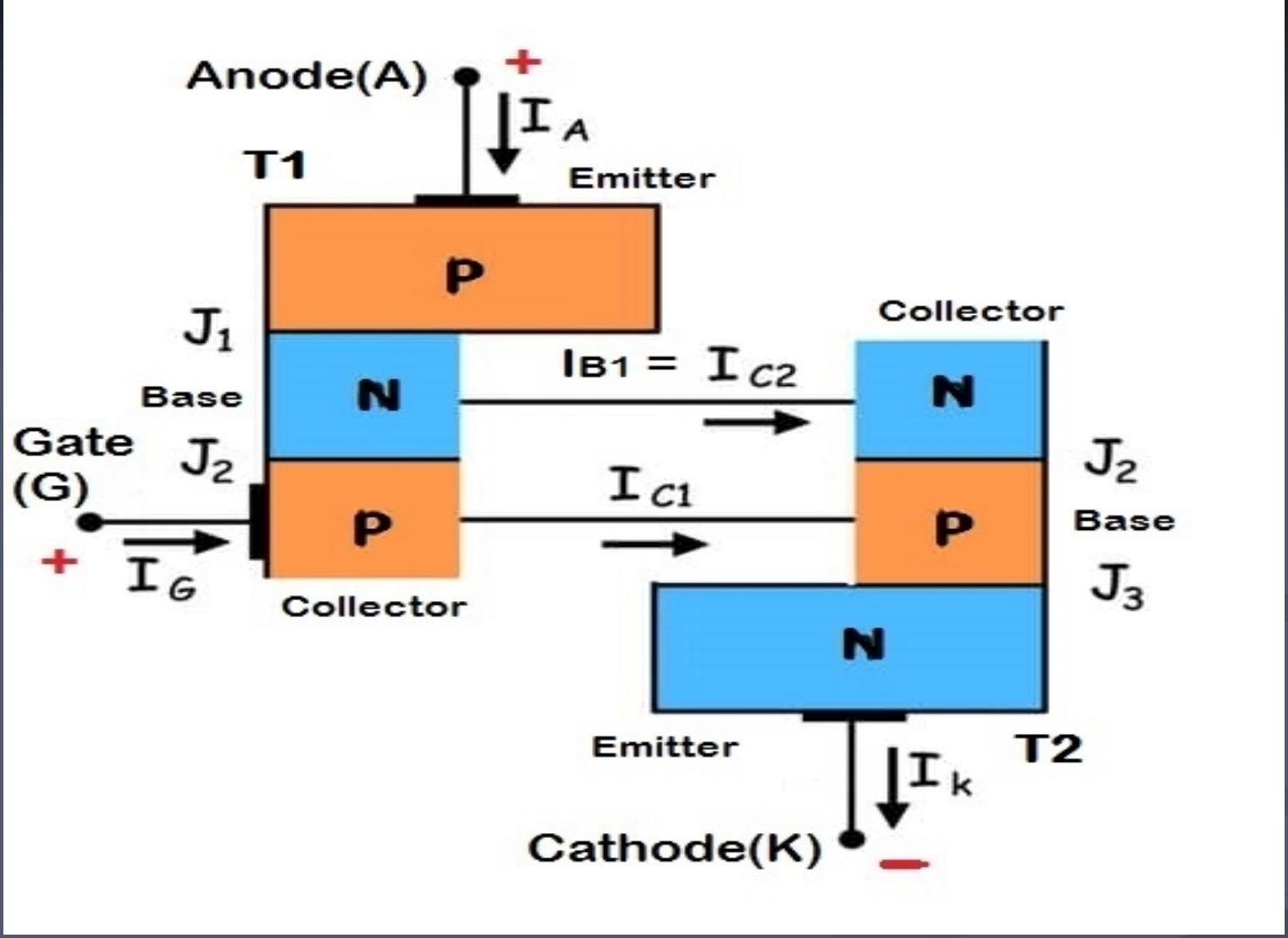
Two Transistor Model of SCR

- The principle of SCR (thyristor) operation can be explained with the use of its Two Transistor Model also called Two Transistor Analogy as it is a combination of P and N layers. **Fig (33)** shows a schematic block diagram of four layers SCR device. It is a four layers PNPN thyristor Device. Imagine the SCR cut along the dotted line, as shown in **Fig (33).** From this **Fig (33),** two transistor model is obtained by bisecting the two middle layers N-type and P-type along the dotted line, in two separate halves as shown in **Fig (34).** Then we can have two devices, as shown in **Fig (34).** These two devices can be recognized as two transistors first one is **PNP type** and second one is **NPN type**.



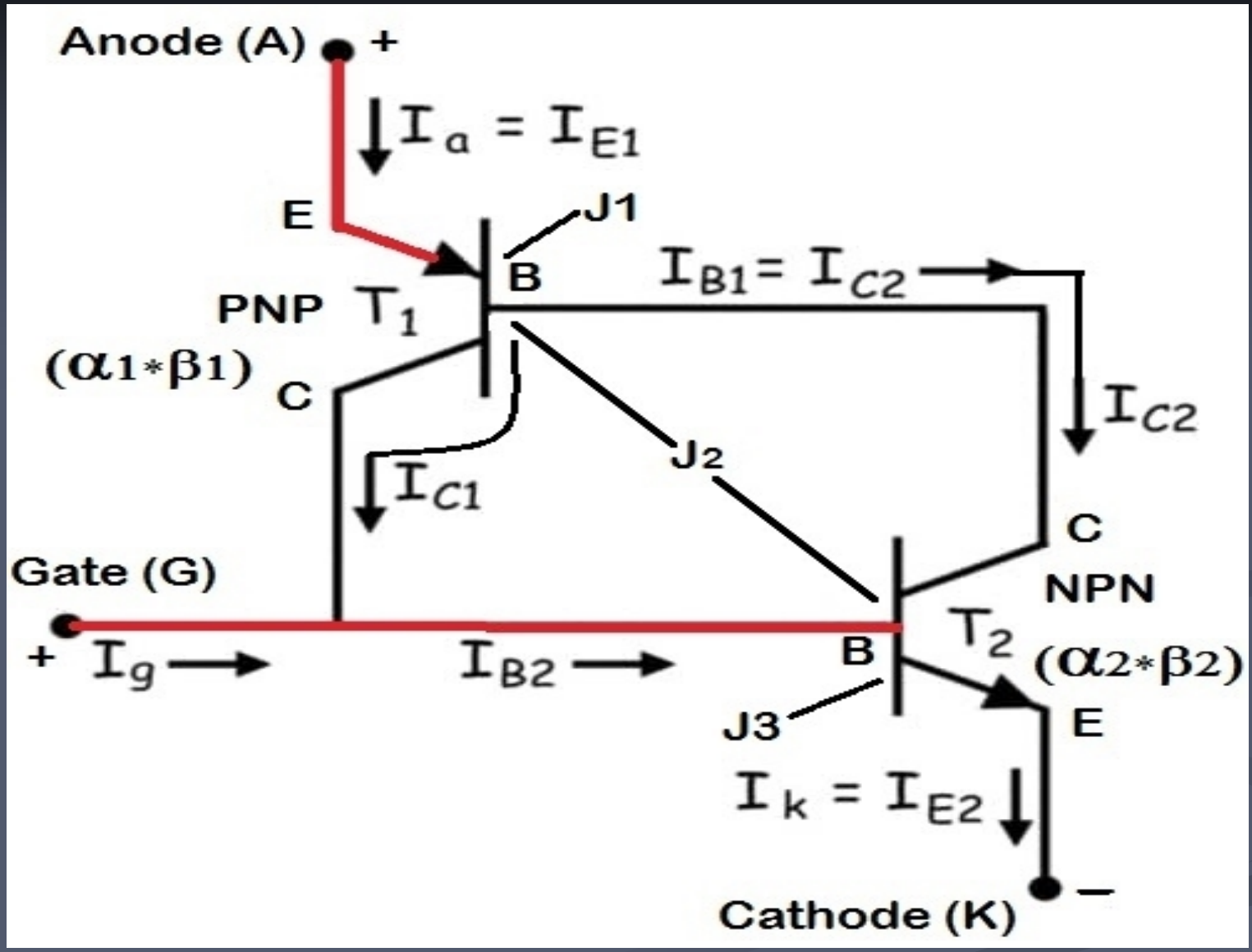
- **Fig (33)** Shown Schematic Block Diagram of SCR cut along the dotted line.

- From **Figure (33),** when we bisect **four layers (P-N-P-N) SCR device** through the dotted line then we will get two transistors i.e. one **PNP transistor** with **J1 and J2** junctions and another is **NPN transistor** with **J2 and J3** junctions. The **upper left** one is **P-N-P type transistor** and the **lower right** one is **N-P-N type transistor.** The **four layers P-N-P-N configuration of SCR** Shown in **Fig (34)** suggests that it can be considered as two coupled transistor. **J1 and J2** form the **Emitter and Collector junction** respectively of a **PNP transistor.** Similarly **J2 and J3** form the **Collector and Emitter junctions** of an **NPN transistor**. In this model (analogy) the **Collector terminal** of the **NPN transistor** is in common with the **Base terminal** of the **PNP transistor** and the **Base terminal** of the **NPN transistor** serve as the **Collector terminal** of the **PNP transistor.** The centre junction J2 serves as the Collector junction for the both transistors.



- **Fig (34)** Shown Two transistor Model is obtained by bisecting the two middle layers along the dotted line, in two separate halves.

- To understand the **SCR Two Transistor Model,** we consider the device as being composed of a **PNP Transistor** and an **NPN transistor** connected in the manner shown in **Fig (34).** Further it can be recognized that the **Base Terminal** of the **P-N-P transistor** is joined to the **Collector Terminal** of the **N-P-N transistor** while the **Collector Terminal** of **P-N-P transistor** is joined to the **Base Terminal** of **N-P-N transistor**, as illustrated in **Fig (34).** The **Gate Terminal** is brought out from the **Base Terminal** of the **N-P-N transistor** and **Collector Terminal** of the **PNP transistor**. **Fig (35) shows the circuit representation of the Two Transistor Model of a SCR.** This construction has been conceived merely to explain the working of SCR; otherwise in physical shape the SCR has four solid layers of P-N-P-N type only.



- **Fig (35)** Shown Two Transistor Model Circuit Diagram of SCR (Thyristor).

- Now we can see from above **Fig (35)** that, the two transistors are connected in such a manner that the **Collector Terminal** of **Transistor T1** is connected to the **Base Terminal** of **Transistor T2** i.e. the output **Collector Current** of **Transistor T1** becomes the **Base Current** for **Transistor T2.** In the similar way the **Collector Terminal** of **Transistor T2** is joined to the **Base Terminal** of **Transistor T1** which shows that the output **Collector Current** of **Transistor T2** is fed to **Transistor T1** as input **Base Current.** These are back to back connections of transistors in such a way that the output of one goes into as input of other transistor and **vice-versa.** This gives net Gain of Loop Circuit as **β1 x β2** where **β1 and β2 are Current Gains of two transistors respectively.**

Theory of Two Transistor Model Operation

- To understand the **SCR Two Transistor Model operation,** we consider When the **Gate (G) terminal** of SCR is **Open-State** means the **Gate Current is zero ($I_g = 0$),** the only current in circulation is the Forward Leakage Current, which is very small in case of silicon device specially and the total current is a little higher than sum of individual Leakage Currents. Under these conditions P-N-P-N device is said to be in its **Forward Blocking Mode (OFF-State) or in High Impedance.**

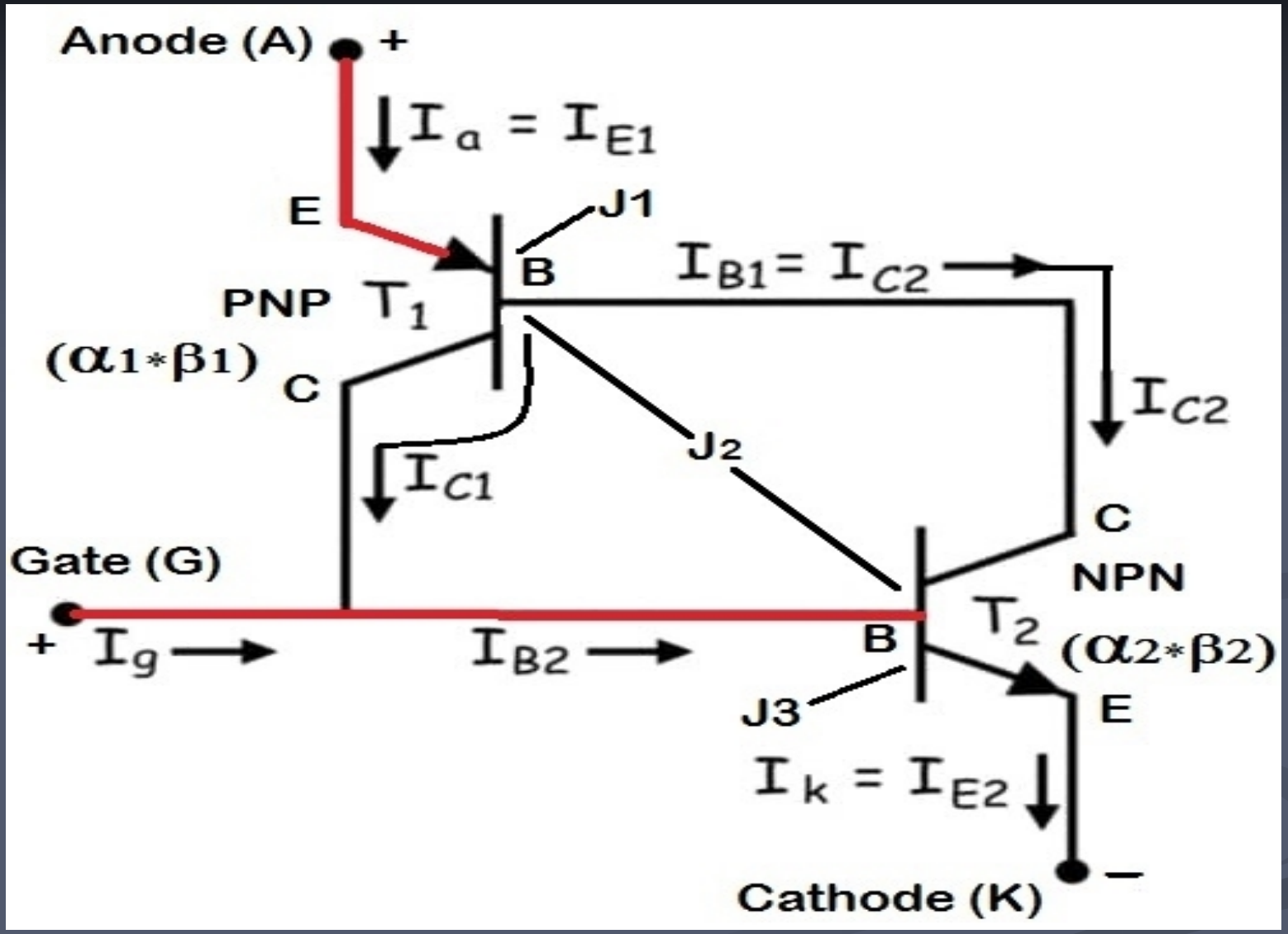
- As soon as Positive (+) Voltage to the Anode (A) with reference to the Cathode (K) and a small amount of **Positive (+) Gate Current (Ig = +ve)** is given to the **Base Terminal** of **Transistor T2** by applying **Forward Bias Voltage** to its **Base-Emitter junction** of **Transistor T2,** it generates the **Collector Current IC2** as **β2 times the Base Current**. This **Collector Current IC2** of **Transistor T2** is fed as input Base Current to **Transistor T1**: which is further multiplied by **β1 times** as **Collector Current IC**1 which forms input **Base Current of Transistor T2** and undergoes further amplification. **In this way both transistors feedback each other and the Collector Current of each goes on multiplying.** This process is very quick and soon both the transistors drive each other to saturation. Now the device is said to be in **ON-State.** The current through the **ON-State SCR** is controlled by **External Load Impedance** only.

- Thus, by applying sufficient Positive (+) Voltage to the Anode (A) with reference to the Cathode (K) and Positive Gate (G) Trigger Pulse, a **Large Anode Current (Ia)** flows through the SCR (thyristor). **This mode of operation of the SCR device is known as the Forward Conduction Mode (ON-State).** In Forward Conduction Mode (ON-State) SCR offers a **Very Low Resistance** to the Large **Anode Current (Ia)** flow. Therefore, the SCR acts as a **Closed Switch (ON-Switch)** in this mode by conducting forward current flowing through the SCR. **Hence, the name of this mode is Forward Conduction Mode (ON-State).**

Analysis of SCR Two Transistor Model (SCR Two Transistor Analogy)

- **The basic operation of a SCR (thyristor) can be explained with the use of its Two Transistor Model also known as Two Transistor Analogy as Shown in Fig (36).** To understand the SCR operation, we consider the SCR device as being composed of a PNP transistor and an NPN transistor connected in the manner shown in **Fig (36).** From **Fig (36)** assume, if **I_{E1}** and **I_{B1}** are the **Emitter Current** and **Base Current** respectively of the **PNP Transistor T1**; **Ia** and **Ik** are the respective **Anode Current** and **Cathode Current** of the **SCR**; **I_{C1}** and **I_{C2}** are the **Collector Current** of **PNP Transistor T1** and **NPN Transistors T2** respectively; **Ig is the Gate Current** of the **SCR**.

- Let us assume that the **Gate (G) terminal is open (Ig = 0)**. Application of a **Forward Bias Voltage** between the **Anode (A) and the Cathode (K) terminal** with the polarity as shown in **Fig (36)** will make the junction **J1 and J3 Forward Biased** and the **junction J2 Reverse Biased.** Assume that the **Current Gain** of the **PNP Transistor T1 is α1** and that of the **NPN Transistor T2 is α2.** The **Collector Current IC1** of the **PNP transistor** derives the **Base terminal** of the **NPN transistor** and the **Base Current IB1** of the **PNP transistor** is directed by the **Collector Current IC2** of the **NPN transistor. The** circuit diagram of the Two Transistor Model of a Four layer P-N-P-N thyristor or Silicon Controlled Rectifier is shown in **Fig (36)** below.



- **Fig (36)** Shown Two Transistor Model Circuit Diagram of SCR (Thyristor).

- In the **OFF-State** of a Transistor, **Collector Current I_C** is related to **Emitter Current I_E** as,

$$I_C = \alpha I_E + I_{CBO} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

- Where,
- α = is the Common Base Current Gain,
- I_{CBO} = is the Common Base Leakage Current at Collector Base junction of a transistor and
- I_E = Emitter Current of transistor.

- **For Transistor T1 from Fig (36),**

- **The Collector Current I_{C1} is given by,**
- **Emitter Current I_E = Anode Current Ia** and
- **Collector Current I_C = I_{C1}**

- Therefore for **Transistor T1,**

$$I_{C1} = \alpha\, Ia + I_{CBO1} \quad \text{..... (2)}$$

- Where,
- $\alpha 1$ = Common Base Current Gain of Transistor T1,
- I_{CBO1} = Common Base Leakage Current of Transistor T1.
- Ia = Emitter Current of Transistor T1.

- Similarly, **For Transistor T2 from Fig (36)**
- **The Collector Current I_{C2} is given by,**
- **Emitter Current I_E = Cathode Current I_k** and
- **Collector Current I_C = I_{C2}**
- Therefore for **Transistor T2,**

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \quad \text{.....} \quad (3)$$

- Where,
- α_2 = Common Base Current Gain of Transistor T2,
- I_{CBO2} = Common Base Leakage Current of Transistor T2,
- I_k = Emitter Current of Transistor T2.

- Now, the sum of two Collector Current given by **Equation (2) and (3)** is equal to the **external circuit current Ia (Anode Current)** entering at Anode (A) terminal of SCR.

$$I_a = I_{C1} + I_{C2}$$

Or, $I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2}$ ..... (4)

- If applied **Gate Current is Ig** then **Cathode Current I_k** will be the summation of **Anode Current (Ia) and Gate Current (Ig)** i.e.

$$I_k = I_a + I_g$$

- Substituting the above value of **Emitter Current Ik** in **Equation (4)** gives,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

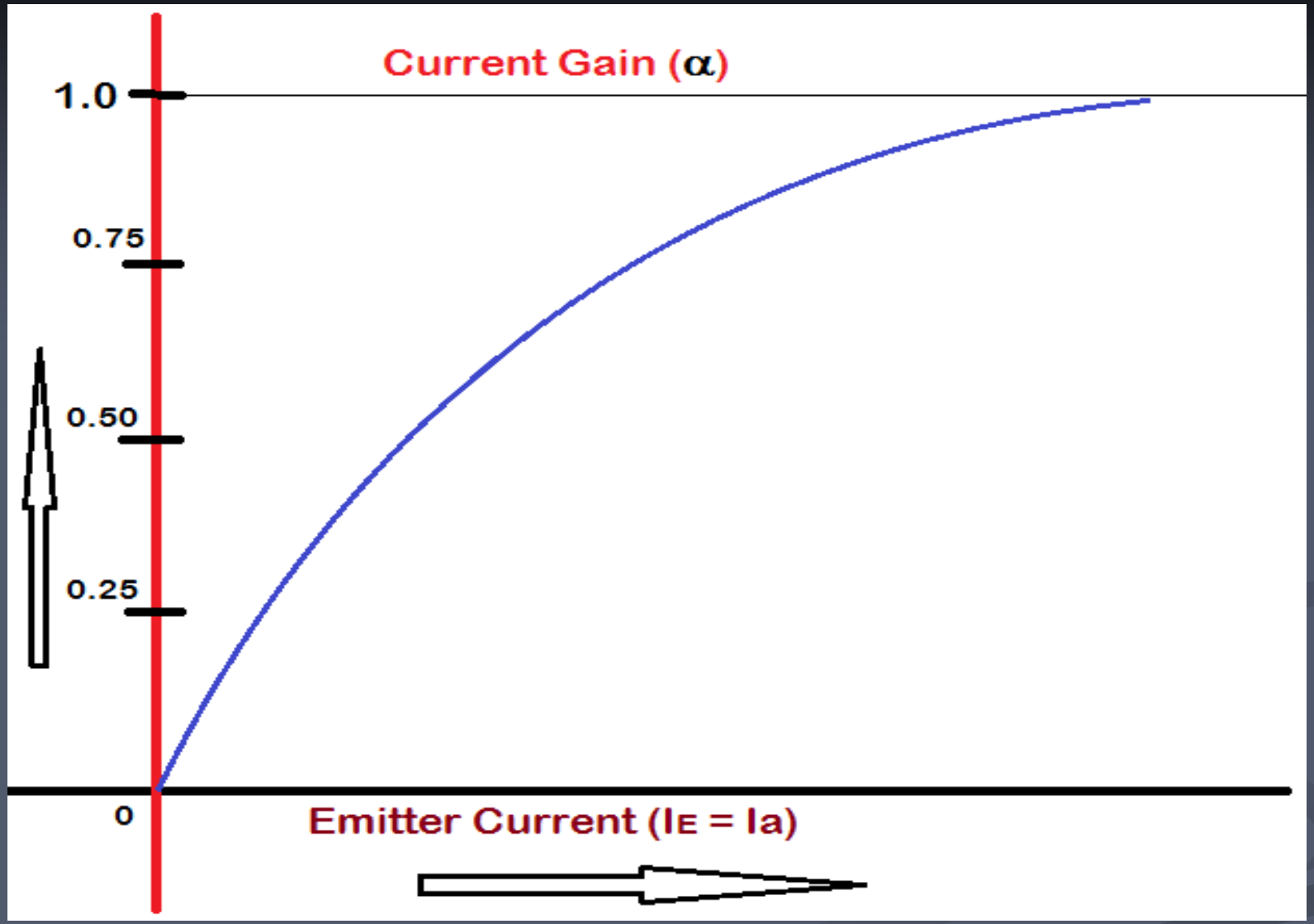
$$I_a = \alpha_2 I_g + I_{CBO1} + I_{CBO2} \;/\; 1 - (\alpha_1 + \alpha_2) \quad \ldots\ldots\ldots\ldots\ldots (5)$$

- By assuming the **Leakage Currents I_{CBO1} and I_{CBO2}** are **negligible** in both **Transistors T1 and T2 then we put $I_{CBO1} + I_{CBO2} = 0$,** we get,

$$I_a = \alpha_2 I_g + 0 \;/\; 1 - (\alpha_1 + \alpha_2)$$

$$I_a = \alpha_2 I_g \;/\; 1 - (\alpha_1 + \alpha_2) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

- For silicon transistor, **Current Gain (α)** is very low at Low **Emitter Current (I_E).** With an increase in **Emitter Current (I_E), Current Gain (α)** build up rapidly as **shown in Fig (37) below.**



- **Fig (37)** Shown Typical Variation of **Current Gain (α)** builds up **with Emitter Current (I_E) of a SCR.**

- Thus, if sufficient Positive (+) Voltage applied to the Anode (A) with respect to the Cathode (K) and with **Gate Current $I_g = 0$, $(\alpha 1 + \alpha 2)$ is Very Low** as per **Equation (5)** and **Forward Leakage Current** somewhat **more than ($I_{CBO1} + I_{CBO2}$) flows through SCR.** If, by some means, the **Emitter Current (I_E)** of two component transistors can be increased, so that **$(\alpha 1 + \alpha 2)$ approaches Unity**, then as per **Equation (5), Anode Current (Ia)** would tend to become **Infinity value thereby Turning- ON the SCR device.**

- After SCR is Turning-ON, all the four layers are filled with carriers and all junctions are Forward Biased. Under these conditions, SCR has very Low Impedance and is in the Forward Conduction Mode (ON-State). **This leads to switching action of the device due to Regenerative Action.** As a consequence, **Anode Current (Ia)** begins to grow (increase) towards a very larger value limited only by **External Load Impedance** to the device. Actually, External Load limits the **Anode Current (Ia)** to a safe value after the SCR (thyristor) begins Conduction. **The methods of Turning-ON a SCR, in fact, are the methods of making ($\alpha 1 + \alpha 2$) to approach unity.**

- **Question :- Now the question is how ($\alpha 1 + \alpha 2$) increasing?**
- **Answer :- Here is the explanation using Two Transistor Model (Analogy) of SCR.**

- When Anode (A) terminal is Positive (+) with respect to Cathode (K) terminal of SCR and with Gate (G) Current $I_G = 0$, then from Equation (4) it shows that Anode (A) Current equal to the Forward Leakage Current, is somewhat more than $I_{CBO1} + I_{CBO2}$. Under these conditions the SCR device is in the Forward Blocking Mode (OFF-State).

- **At the first** stage when we apply a **Gate Current (Ig = + ve),** a sufficient **Gate-Drive Current** between Gate (G) and Cathode (K) terminal of the transistor is applied. Then, this **Gate-Drive Current (Ig)** is equal to **Base Current $I_{B2} = I_g$** and **Emitter Current I_{E2}** of **Transistor T2** is **$I_{E2} = I_k$.**

- With the establishment of **Emitter Current $I_E = I_k$** of **Transistor T2**, **Current Gain $\alpha 2$** of **Transistor T2** increase as,

$$\alpha 2 = I_{CBO1} / I_g$$

- And **Base Current I_{B2}** causes the generation of **Collector Current I_{C2}**

$$I_{C2} = \beta 2\ I_{B2} = \beta 2\ Ig.$$

- **This amplified Collector Current I_{C2}** serves as the **Base Current I_{B1}** of **Transistor T1.** With the flow of **Base Current I_{B1}**, this will cause the flow of **Collector Current I_{C1}** of Transistor T1 comes into existence.

$$I_{C1} = \beta 1\ I_{B1} = \beta 1 \beta 2 Ig$$

- **Current I_{B1} and I_{C1}** lead to the establishment of **Emitter Current Ia** of **Transistor T1** and this causes **Current Gain $\alpha 1$** to rise as desired.

- Now Current,

  $$I_g + I_{C1} = (1 + \beta_1 \beta_2)\, I_g$$

- acts as the **Base Current I_{B2}** of **Transistor T2** and therefore its **Emitter Current $I_k = I_{C1} + I_g$.**

- With the rise in **Emitter Current IK**, **Current Gain α_2 of Transistor T2** increases and this further causes **Collector Current I_{C2}** to increases as,

  $$I_{C2} = \beta_1 (1 + \beta_1 \beta_2)\, I_g$$

- As amplified **Collector Current (I_{C2})** is equal to the **Base Current (I_{B1})** of **Transistor T1**

  $I_{B1} = I_{C2}$.

- **Therefore, Current Gain $\alpha 1$** eventually **increases further.**

- **There is thus established a Regenerative Action internal to the SCR device. This Regenerative or** Continuous **Positive Feedback Effect causes ($\alpha 1 + \alpha 2$) to grow towards Unity.** As a consequence, **Anode Current (Ia)** begins to **grow (increase)** towards a very larger value limited only by **External Load Impedance** in the external circuit. In other word, the SCR device suddenly **Latches into Conduction State from the original Non-Conducting State.** The reason for such behaviour is the **Regenerative manner** in which the two **transistors T1 and T2** are interconnected. When **Regeneration has grown sufficiently,** Gate current can be withdrawn. Even after **Positive (+) Gate Current (Ig = +ve) is removed, Regenerative Action continues.** Thus if the **Gate Current Ig** is of such a magnitude that **($\alpha 1 + \alpha 2$) = 1,** the SCR will be triggered. This characteristic of the SCR makes is suitable for Pulse Triggering.

- The value of **($\alpha 1 + \alpha 2$) can be made** almost Unity by a **Positive Gate Current** of proper magnitude and for short duration at the Gate Terminal. Signal **Gate Current Ig** when applied to the **Gate Terminal** causes a flow of **current** in **Transistor T2.** This gives rise to the **Collector Current I_{C2} in Transistor T2.** Now the **Transistor T1 Base Terminal** is energized because its **Base Current** is the **Collector Current** of **Transistor T2** and so the **First Transistor T1 is switched ON.** Thus each of the Transistor **supplies Base Current** to the other and action therefore, **Regenerative Action.** At this point even if the **Gate signal is removed**, the **SCR device does not Turn-OFF as long as the magnitude of the current flowing does not fall below that of Holding Current.**

- It implies that when the **SCR** device is **Forward Biased** it can be triggered by applying a small duration **Positive Pulse** at the **Gate Terminal.** Once the **SCR device Latches into the Conduction State,** the **Gate loses its control** and the **SCR device remains in the Conducting State,** even if the **Gate is Opened,** till the current level is maintained to the minimum of that of the Latching Current.

- Now, even if we **remove the Positive (+) Gate Voltage** then **Regenerative Feedback Action** will take place and the **Maximum Forward Current or Forward Anode Current (+Ia)** flows through the SCR device once it reaches the **Minimum Current value.**

- **This Minimum Current is known as Latching Current (I_L).** We know that SCR is a Latching Device. Here the **Latching Current (I_L)** is defined as the minimum current required to maintain the SCR in **Conducting State (ON-State)** even after the **Positive (+) Gate Voltage (Gate Pulse Ig = + ve)** is removed. In such state, the **SCR is said to be Latched** and there will be no means to limit the **Maximum Forward Current flowing through the SCR device,** and limited only by **External Load Impedance** in the external circuit. After SCR is **Turning-ON,** all the four layers are filled with carriers and all junctions are Forward Biased. Under these conditions, SCR has very low impedance and is in the **Forward Conduction Mode (ON-State).**

- When **($\alpha 1 + \alpha 2$) becomes appreciably** less then Unity, the **Anode Current Ia,** from **equation (4) and (5),** becomes extremely small and the SCR device is said to be in the **OFF-State or Non-Conducting State.** On the other hand with **($\alpha 1 + \alpha 2$) = 1,** the **Anode Current Ia** is **extremely large and the device is said to be in the ON-State or Conducting-State.** In **Conducting State**, the **Voltage Drop across the SCR device drops to a Low value and a Large Anode Current flows through SCR** and its value limited only by the **External Resistor** in the external circuit. Thus the existence of the **SCR** either in the **ON -State** or in the **OFF-State** depends on the applied **Anode Voltage** with reference to **Cathode** and the **Gate voltage.**

- to be continued .....