TOPIC: FIELD EFFECT TRANSISTOR

UG-III

The field effect transistor is a semi-conductor device in which the output current is controlled by an electric field. Since only one type of carrier, specially majority carriers, are involved in the operation of FET it is termed as a "unipolar transistor."

There are two main classes of field effect transistors

(A) Junction field-effect Transister (JFET)

(B) Metal oxide semi-conductor field-effect transistor (MOSFET).

JUNCTION FIELD EFFECT TRANSISTOR

Fig (1) shows a junction field-effect transistor. It consists of a uniformly doped semiconductor bar (channel) with ohmic contact at both ends and with semiconductor junctions on both sides of the bar. The semiconductor bar may be of n-type material or of p-type material. In the former case, the JFET is termed an n-channel FET whereas for the p-type bar, it is called a p-channel FET. The junction on both sides of the bar are formed with impurities opposite to that of the channel. Current is allowed to

flow along the length of the bar by applying a voltage between the end terminals of the bar. The current is carried by majority carriers which drift through the channel. Silicon and sometimes gallium arsenide are usually taken as the basic semiconductors for the FETs. The different notations marked on the figure are

Source (S): The terminal through which the majority carriers enter the channel.

Drain (D): - The terminal through which the majority carriers leave the channel.

Gate (G): - On both side of the doped semi-conductor bar heavily doped region are formed by alloying, diffusion or by other techniques using impurities opposite to that of the channel. These regions are called the gate.

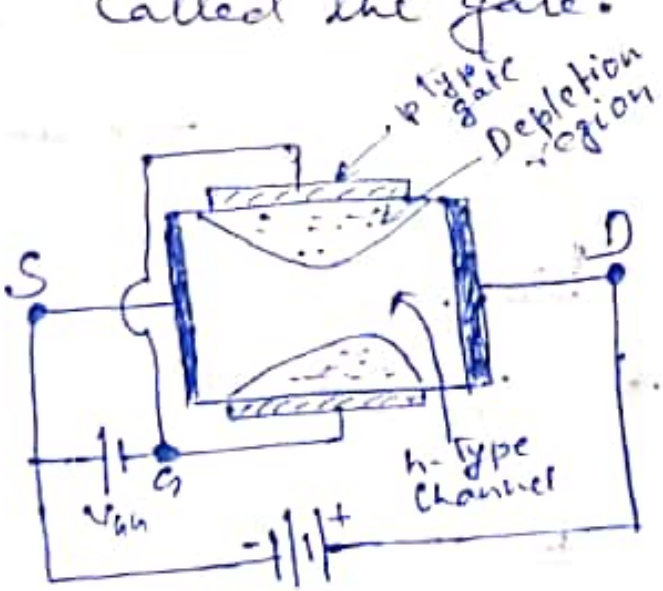


Fig (1)

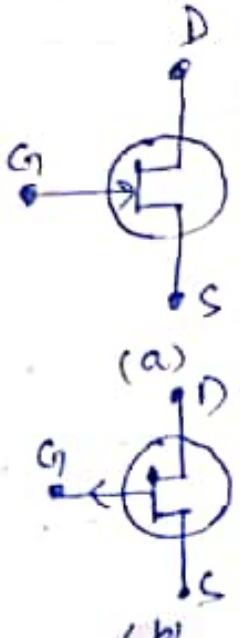


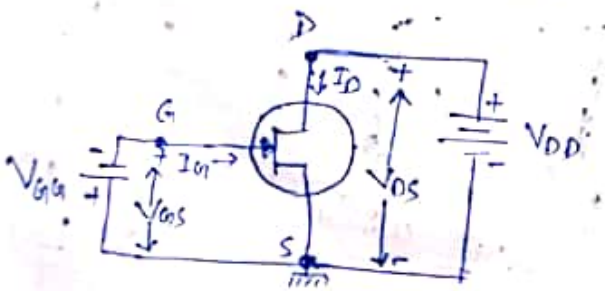
Fig (2)

SYMBOLIC REPRESENTATION OF FET

The circuit symbols of n-channel and p-channel FETs are shown in fig(2a) & (2b) respectively. The arrow on the gate terminal refers to the direction of the gate current when the gate-source junction is forward biased. However, in normal operation, the gate-source junction is reversed-biased.

A schematic diagram of an n-channel FET with its terminals connected properly to voltage source is shown in fig (3). The source voltages V_{GG} and V_{DD} respectively supply the gate voltage and the drain voltage. The actual sign of various currents and voltages for the n-channel FETs are as follows

I_D = +ve, I_G = -ve, V_{DS} = +ve and V_{GS} = -ve



fig(3)

PRINCIPLE OF OPERATION

When the junction between the gate and the source is reverse-biased there will be depletion regions on both sides of the channel. These depletion regions will extend into the channel as the reverse-bias voltage is increased. The depletion regions contain only immobile charges and no free carriers; therefore, the conductivity of these regions will be practically zero. Hence the effective cross section of the conducting channel between the depletion regions will decrease with increase in the reverse-bias voltage. Thus for a fixed drain-to-source voltage, the drain current will be a function of the gate-to-source voltage. In other words, the voltage applied to the gate controls the drain current & hence the name "Field Effect Transistor."