Paper 7, TDC Part-3
Chapter– 1, Fundamental Concept of Digital Electronics
Lecture - 3

By:

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Fundamental Concepts of Digital Electronics

In last two lectures we have discussed three basic gates: “NOT” Gate, “OR” Gate and “AND” Gate. These basic gates can be used to realized any digital circuits or in other words we can say that any logic (Boolean) expression can be realized using these basic gates.

From these 3 basic gates we can derive two more gates. These derived gates are “NAND” and “NOR” gates. “NAND” gate and “NOR” gate are known as universal gates.

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We can realize any logical expression or design any digital circuits using only one type of gates, either “NAND” or “NOR” Gate. In other words we will say as below:-

Only “NAND” gate is sufficient for the realization of any logical expression.

Or

Only “NOR” gate is sufficient for the realization of any logical expression.

Due to this reason “NAND” and “NOR” gates are called universal gates.

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- **The NAND Logic : -**

The NAND logic (operation) is a combination of two basic logics, the NOT & AND logics. This means that the output of the NAND logic is the inverted (complement) output of AND logic.

The NAND operation is defined as:- When all the inputs are at logic “1” then the output is at logic “0” else the output is at logic “1”. The NAND Gate can have N numbers of inputs $(N \geq 2)$ and One output.

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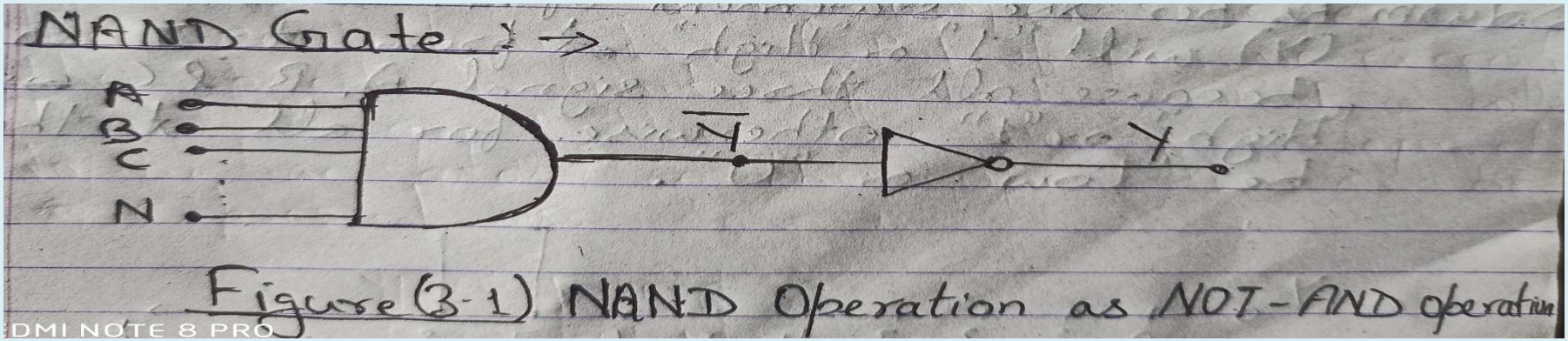
The logical expression of NAND operation is given by

$$Y = \overline{A \text{ AND } B \text{ AND } C \text{ AND } \ldots\ldots\ldots\ldots \text{ AND } N}$$

$$Y = \overline{A \cdot B \cdot C \cdot \ldots\ldots\ldots\ldots\ldots \cdot N}$$

$$Y = \overline{ABC \ldots\ldots\ldots N}$$

- **<u>Symbol for NAND Gate : -</u>**



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- **Symbol for NAND Gate : -**

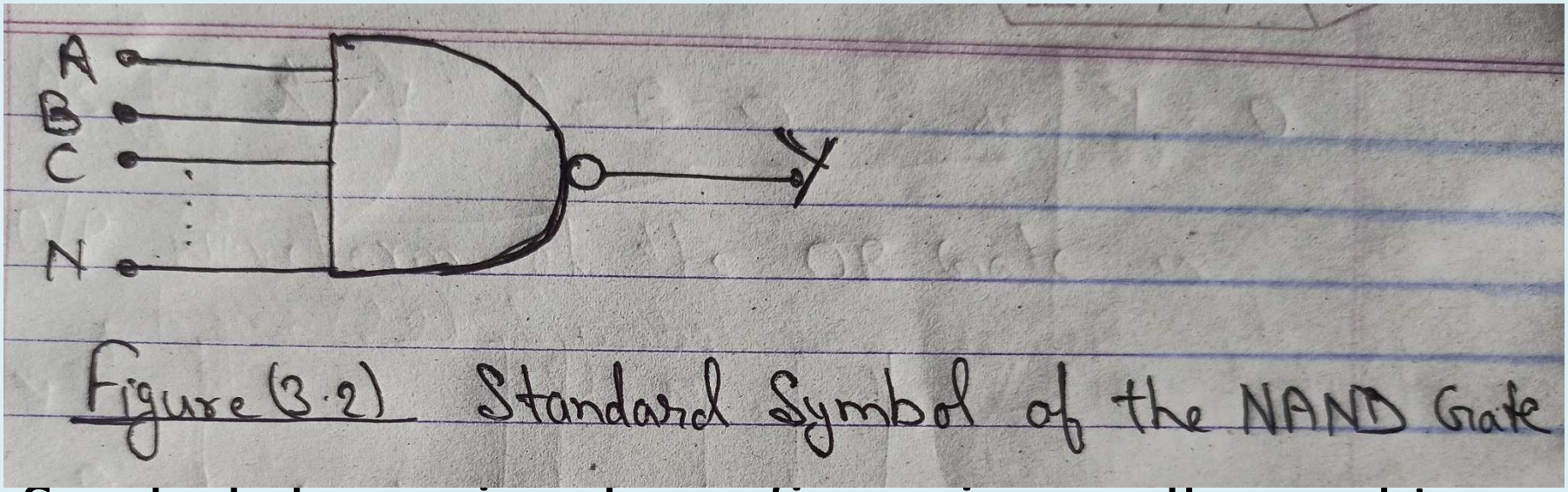

Figure (3.2) Standard Symbol of the NAND Gate

Symbol shown in above figure is usually used to represent “NAND” gate.

A bubble on the output side of the “NAND” gate represent “NOT” operation.

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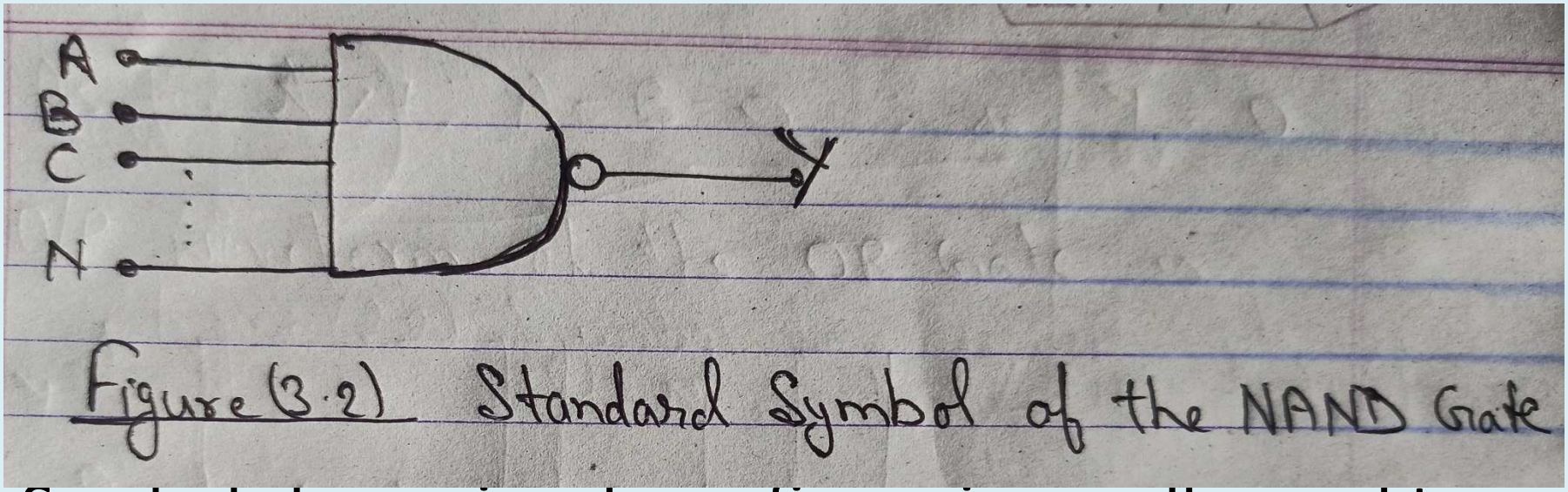
- **Symbol for NAND Gate : -**



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A bubble on the output side of the “NAND” gate represent “NOT” operation.

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- **Logic Equation & Truth Table for NAND Gate : -**
  - **2 input NAND Gate**

Logic equation for 2 input NAND gate is:-

$$Y = \overline{A\ B}$$

Input (A)	Input (B)	Output (Y)
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table for 2- Input NAND Gate

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- **3 input NAND Gate**

Logic equation for 3 input NAND gate is:-

$Y = \overline{A\ B\ C}$

Input (A)	Input (B)	Input (C)	Output (Y)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table for 3 Input NAND Gate

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Similarly the truth table of a NAND Gate with any numbers of input signals can be written. The output of a NAND Gate will be “Low (0)” when all the input signals are “High (1)” otherwise for any other combinations of inputs signal, the output will be “High (1).

All three basic gates, “NOT”, “OR” & “AND” gate can be realized using “NAND” Gate

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Implementation of NOT Gate using NAND Gate

As we have seen earlier that NOT Gate complement / Invert the logic state of the input signal so we can implement NOT Gate using NAND Gate as below

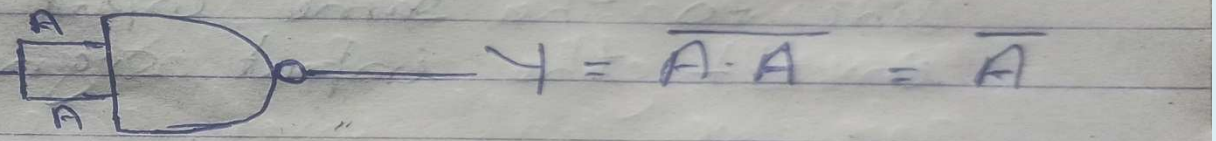

Fig (3.3) → NOT gate using NAND gate

The above operation can be understand from the truth table of NAND Gate also

I/P = A	I/P A	O/P = Y
0	0	1
1	1	0

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So to implement a NOT gate using NAND gate we will short all input line of the NAND gate and provide the input signal. By this all the input line will have the same signal ~~just like~~ i.e. only one input just like a "NOT" gate which has only one input. As we can see from the ~~table~~ truth table, by this connection we will get inverted (complement) input signal at the output line.

So we can convert ~~any~~ N-input "NAND" gate to a "NOT" gate by connecting all its input line to the same input signal. This will invert the input signal.

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So we can convert ~~any~~ N-input "NAND" gate to a "NOT" gate by connecting all its input line to the same input signal. This will invert the input signal.

Implementation of "OR" Gate using NAND Gate :→

2 I/P "OR" Gate "

For 2 I/P "OR" Gate O/P is

$$Y = \overline{\overline{A}\,\overline{B}} \cdot A + B$$

The above equation can be written as below also.

$$Y = \overline{\overline{A+B}}$$

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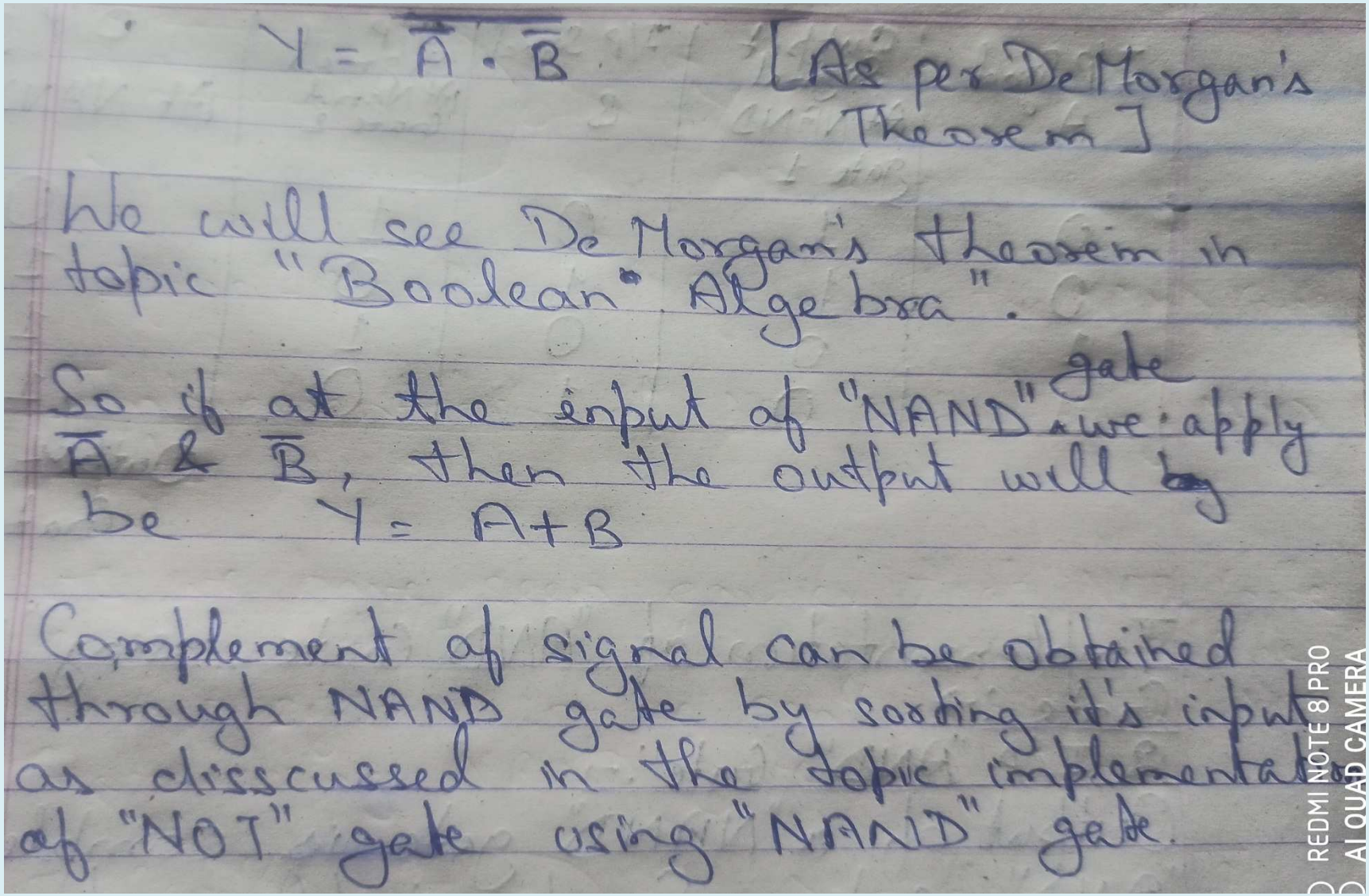

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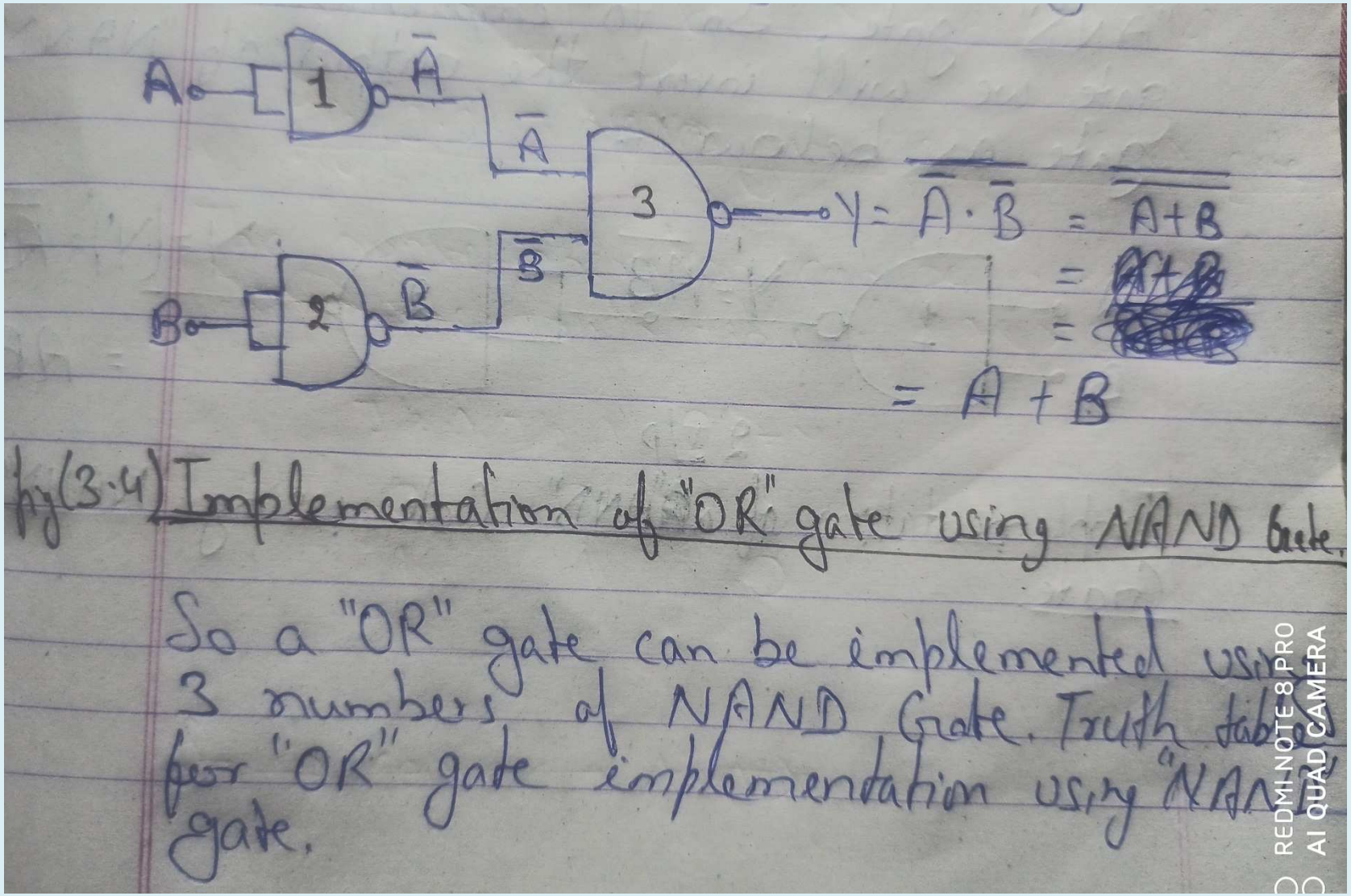

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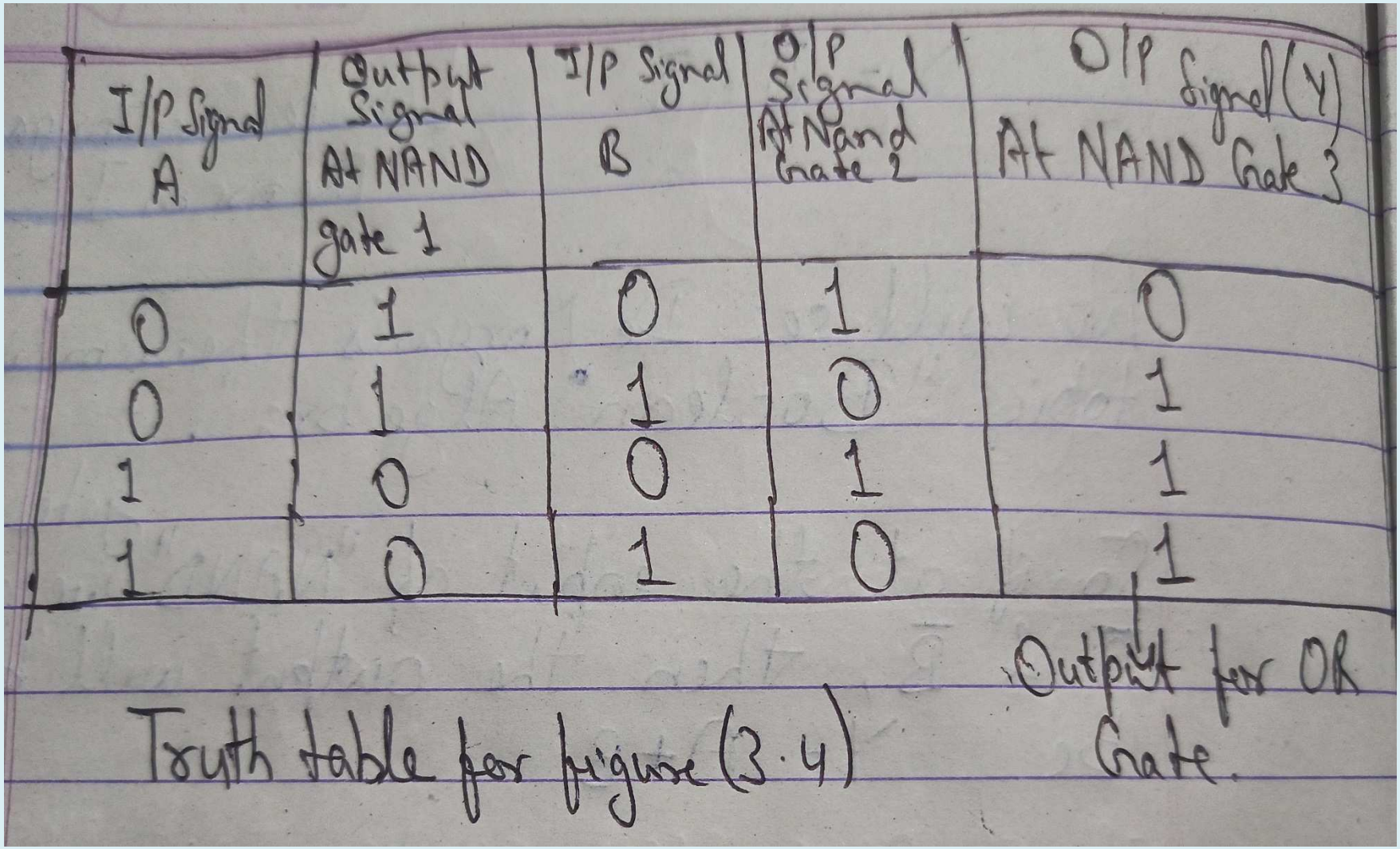

I/P Signal A	Output Signal At NAND gate 1	I/P Signal B	O/P Signal At Nand Gate 2	O/P Signal (Y) At NAND Gate 3
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1

Output for OR Gate.

Truth table for figure (3.4)

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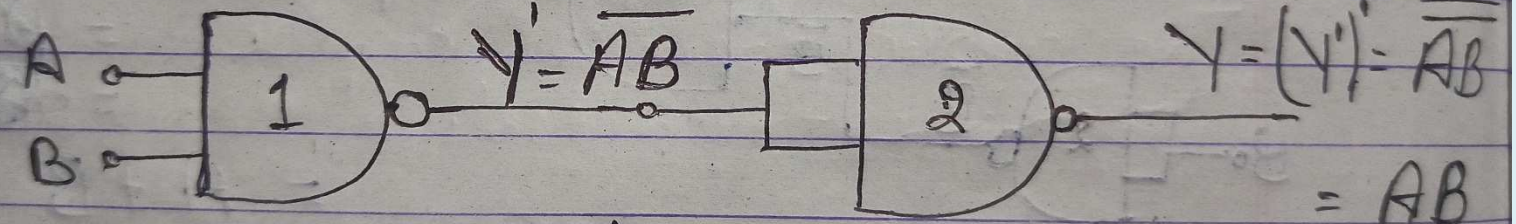
Implementation of "AND" Gate using "NAND" Gate :→

2 I/P "AND" Gate :→

Output of a "NAND" gate is complement of "AND" gate. So to implement a "AND" gate we will invert the output of "NAND" gate as below :→



2 I/P

fig(3.5) Implementation of "AND" Gate using "NAND" Gate

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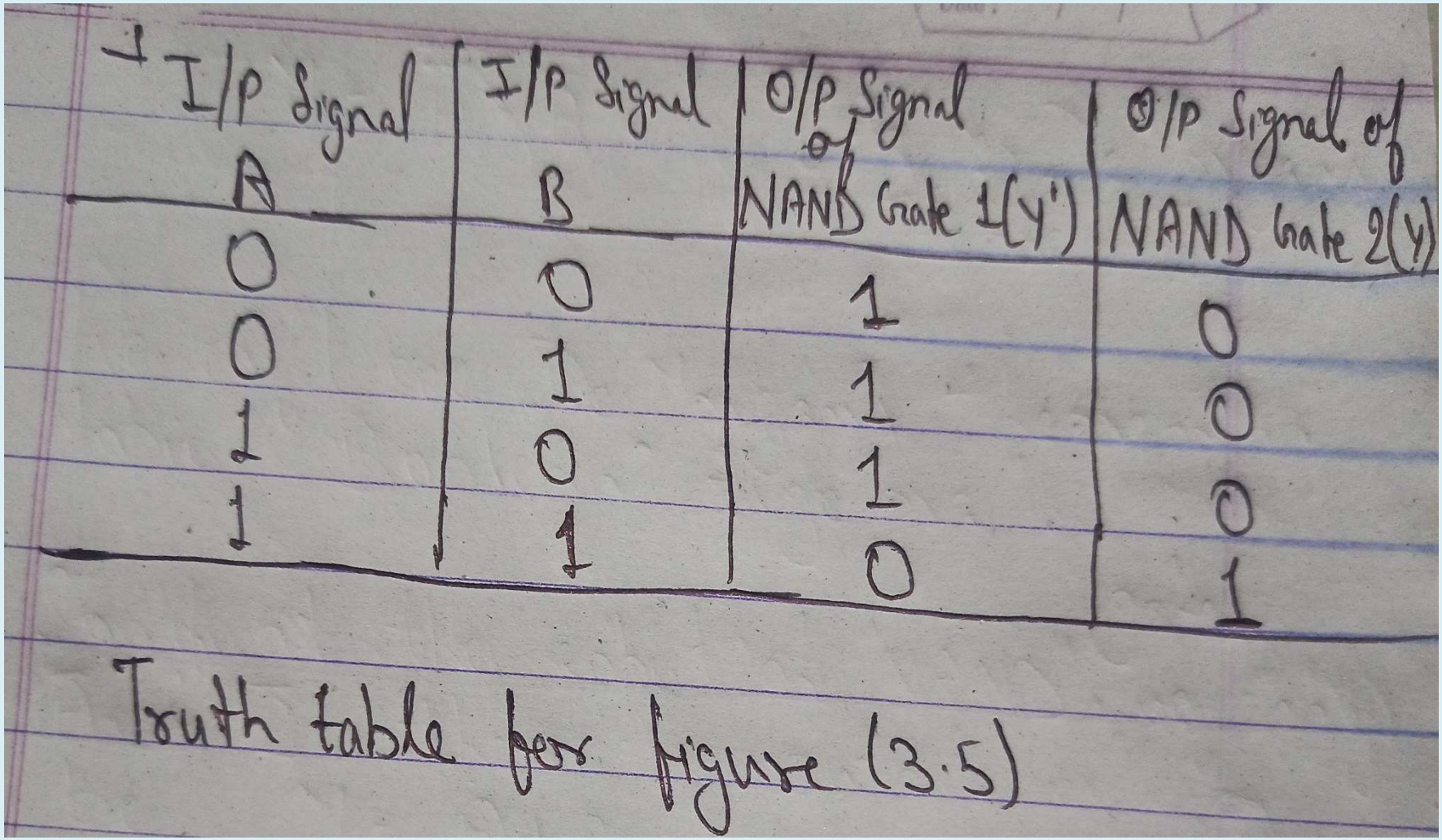

I/P Signal A	I/P Signal B	O/P Signal of NAND Gate 1(Y')	O/P Signal of NAND Gate 2(Y)
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table for figure (3.5)