⇒ Conversion of NAND ckt. into OR, AND & NOT circuits:

A NAND-gate can be used to build an OR, AND, or a NOT ckt. when all inputs of a NAND gates are connected together a NOT-gate results shown in fig. 6(a), because if A = 1, the output of a NAND gate is $\overline{A} \cdot \overline{A} = \overline{1} \cdot \overline{1} = \overline{1} = 0$ and if A = 0, the output is $\overline{A \cdot A} = \overline{0 \cdot 0} = \overline{0} = 1$.

Fig. 6(a) NOT-gate from NAND gate.

→ **AND CKt:-** A NAND-gate followed by NOT ckt is an AND gate. shown in fig. 6(b).

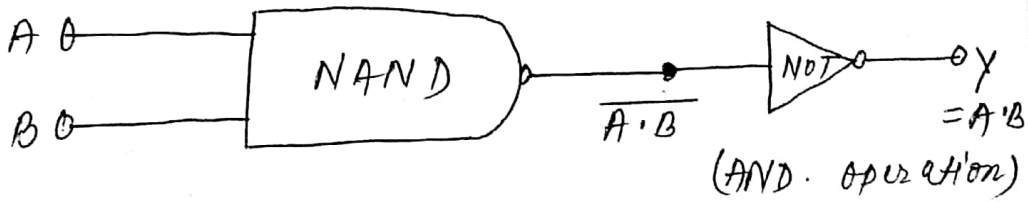

Fig. 6(b): AND from NAND & NOT.

AND-gate can also be obtained by using two NAND-gates repeatedly fig. 6(c). The output of two inputs NAND-gate is fed to single input.

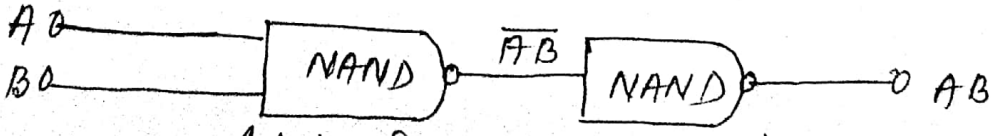

Fig. 6(c) Double NAND's is a AND.

is NAND gate, Hence

$\overline{A \cdot B} = A \cdot B$ which is output of an AND gate

→ **OR GATE:** OR gate fig 6-(d) from NAND gate is obtained by using two single input NAND gates and one, two inputs NAND gate.

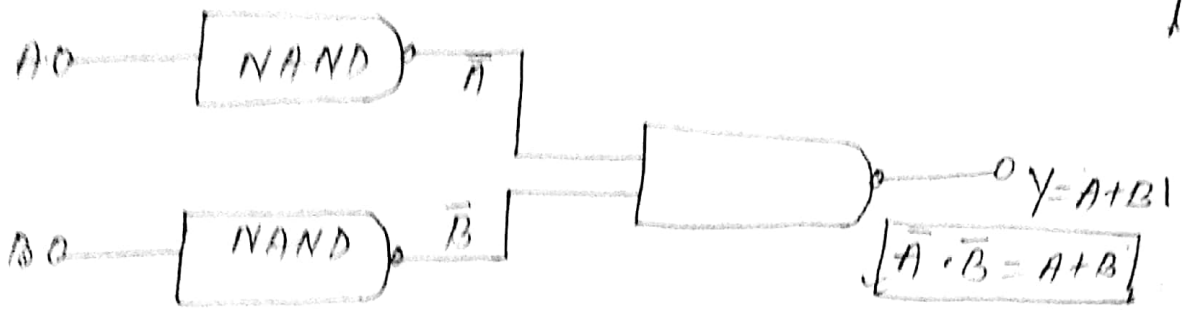

Fig. 6-(d).

First two NAND's convert A & B into $\overline{A}$ & $\overline{B}$. The 2nd two inputs NAND gives $\overline{A} \cdot \overline{B} = \overline{\overline{A}} + \overline{\overline{B}}$ $= A + B$, which is OR-gate. OR-gate can also be obtained by connecting two NOT output to two inputs of a NAND GATE shown fig. 6(e).

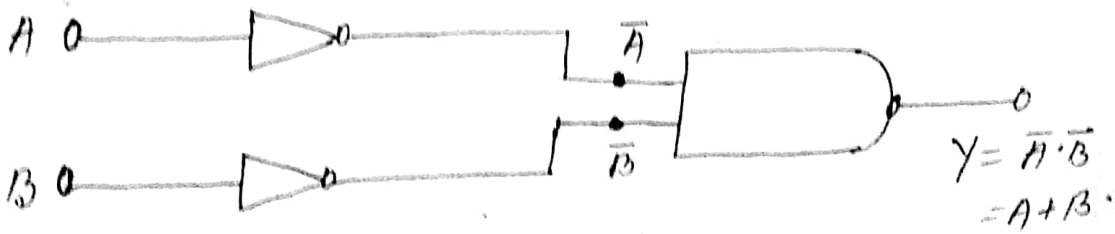

Fig. 6-(e) OR gate from 1 NAND & two NOT