

Paper 7, TDC Part-3
Discussion of some questions of 2017
Lecture - 2

By:

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Discussion of 2017 Questions

Q3) Given the logic equation:

$$f = ABC + B\bar{C}D + \bar{A}BC$$

- Make a truth table
- Simplify using K-map.
- Realize f using NAND gates only.

Soln: The function f is a logic function of 4-variables A, B, C, D , so there are total of 16 combinations are possible. Truth table for $f = ABC + B\bar{C}D + \bar{A}BC$

A	B	C	D	ABC	$B\bar{C}D$	$\bar{A}BC$	f
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0

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Contd.

A	B	C	D	ABC	$B\bar{C}D$	$\bar{A}BC$	f
0	1	0	0	0	0	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	1

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(b) Simplify logic function f using K-map, since the logic function is 4-variable function so we draw K-map with 16 cells as below and enter the true value of logic function in respective cell.

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

→ BC

↓ BD

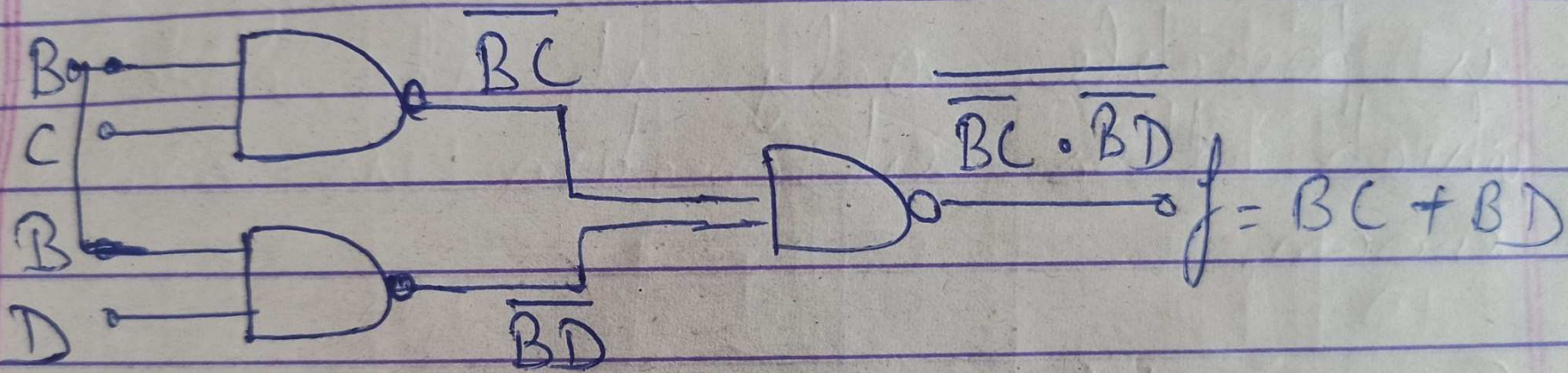
$$f = BC + BD$$

(c) Realising the ~~circuit~~ ^{simplified} ~~using~~ logic function f using

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NAND gates only

$$f = BC + BD = \overline{\overline{BC + BD}} = \overline{\overline{BC} \cdot \overline{BD}}$$



Realising $f = ABC + B\bar{C}D + \bar{A}BC$ using NAND gates only.

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Q7) Design an excess-3 to BCD converter using minimum number of NAND gates?

In BCD (Binary Coded Decimal) code, decimal digit of 0 through 9 are represented by their natural binary equivalents using 4-bits and each decimal digit of a decimal number is represented by the 4-bit code individually. For example $(52)_{10}$ is represented as $(0101\ 0010)$ in BCD code. BCD code is also known as

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Excess-3 code is another form of BCD code, in which each decimal digit is coded into a 4-bit binary code. The code for each decimal digit is obtained by adding decimal 3 to the natural BCD of the digit.

For example decimal 5 is coded as ~~0101~~
 $(0101 + 0011) = 1000$ in Excess 3-code.

To design an Excess-3 to BCD converter we first write table as below

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E ₂	Excess 3			D	C	B	A
	E ₀	E ₁	E ₃				
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

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Handwritten Karnaugh maps for variables A and B on lined paper.

A =

$E_3 E_2 \backslash E_1 E_0$	00	01	11	10
00	X	X	..	X
01	1			1
11	1	X	X	X
10	1			1

B =

$E_3 E_2 \backslash E_1 E_0$	01	11	10
00	X	X	X
01	1		1
11	X	X	X
10	1		1

Below the Karnaugh maps, the simplified Boolean expressions are given:

$A = \bar{E}_0$

$B = \bar{E}_1 E_0 + E_1 \bar{E}_0$

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Handwritten Karnaugh maps and Boolean expressions for variables C and D.

Map C:

$E_3 E_2$	$E_1 E_0$	00	01	11	10
00		X	X		X
01				1	
11		X		X	
10					1

Groupings for C:
 - A group of four cells (00, 01, 10, 11) in the first row is circled, leading to the expression $\bar{E}_2 \bar{E}_1 + \bar{E}_2 \bar{E}_0$.
 - A group of two cells (01, 11) in the second column is circled, leading to the expression $E_2 E_1 E_0$.

Map D:

$E_3 E_2$	$E_1 E_0$	00	01	11	10
00		X	X		X
01					
11		1	X	X	X
10					

Groupings for D:
 - A group of four cells (00, 01, 10, 11) in the first row is circled, leading to the expression $E_3 E_2$.
 - A group of two cells (11, 10) in the fourth row is circled, leading to the expression $E_3 E_1 E_0$.

Final Boolean expressions:

$$C = \bar{E}_2 \bar{E}_1 + \bar{E}_2 \bar{E}_0 + E_2 E_1 E_0$$

$$D = E_3 E_2 + E_3 E_1 E_0$$

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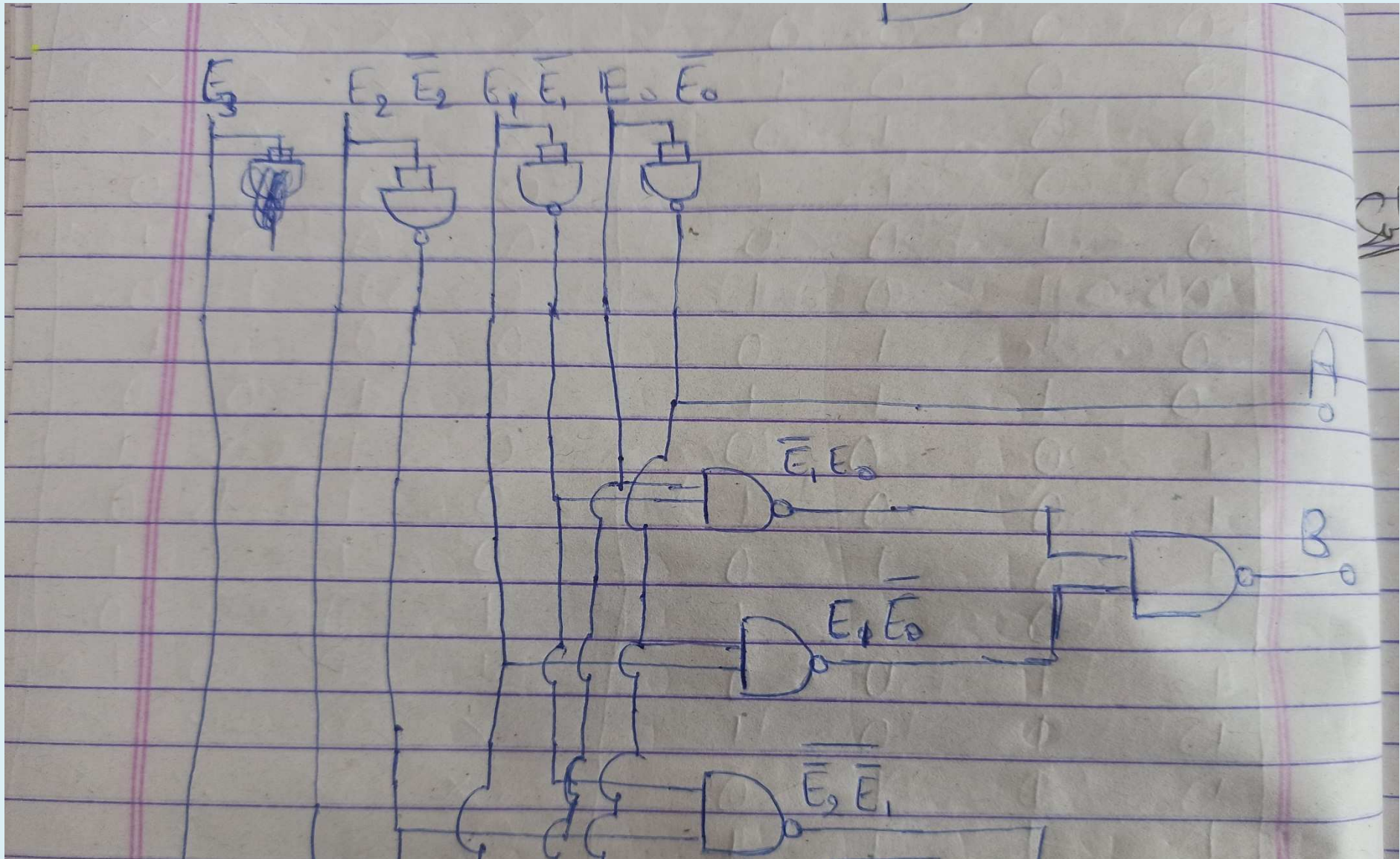
For designing using minimum number of NAND gates only we write,

$$B = \overline{\overline{E_1 E_0}} + \overline{\overline{E_1 \overline{E_0}}} = \overline{\overline{E_1 E_0}} \cdot \overline{\overline{E_1 \overline{E_0}}}$$

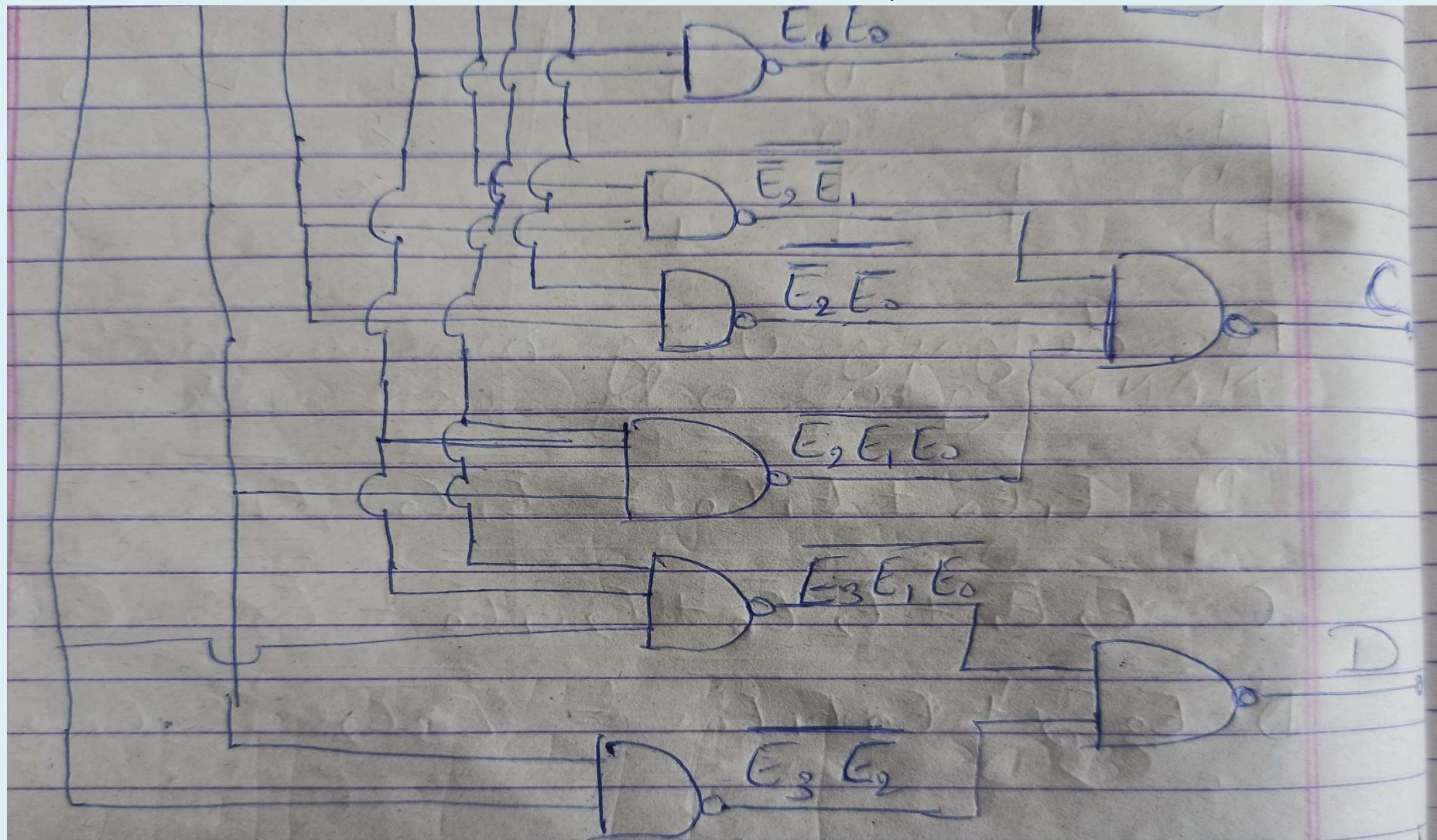
$$C = \overline{\overline{\overline{E_2} \overline{E_1}}} + \overline{\overline{\overline{E_2} \overline{E_0}}} + \overline{\overline{\overline{E_2} E_1 \overline{E_0}}} = \overline{\overline{\overline{E_2} \overline{E_1}}} \cdot \overline{\overline{\overline{E_2} \overline{E_0}}} \cdot \overline{\overline{\overline{E_2} E_1 \overline{E_0}}}$$

$$D = \overline{\overline{\overline{E_3} \overline{E_2}}} + \overline{\overline{\overline{E_3} \overline{E_1} \overline{E_0}}} = \overline{\overline{\overline{E_3} \overline{E_2}}} \cdot \overline{\overline{\overline{E_3} \overline{E_1} \overline{E_0}}}$$

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Free 3 to BCD converter using NAND gates

Combinational Logic Design

Refer book- Modern Digital Electronics by RP Jain.

Thank You