

Paper 7, TDC Part-3
Discussion of some questions of 2017
Lecture - 25

By:

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Discussion of 2017 Questions

Discussion of a Few Questions of "2017"
Paper - 7 (VII)

(1.) Prove the following using De Morgan's Theorem:

$$(a) \quad AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$$

$$(b) \quad \overline{(A+B) \cdot (C+D)} = \overline{(A+B)} + \overline{(C+D)}$$

Hence prove the following statements:

(a) An AND-OR configuration is equivalent to a NAND-NAND configuration.

(b) An OR-AND configuration is equivalent to a NOR-NOR configuration.

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Soln. → 1(a) $AB + CD$

Let $AB = X$ & $CD = Y$
then above function can be written as

$$AB + CD = X + Y = \overline{\overline{X + Y}} \quad [A, \overline{\overline{A}} = A]$$

$$= \overline{\overline{X} \cdot \overline{Y}} \quad [A \text{ per De Morgan's Theorem } \overline{A + B} = \overline{A} \cdot \overline{B}]$$

~~Soln~~ Now putting value of X & Y we get.

$$AB + CD = \overline{\overline{AB} \cdot \overline{CD}} \quad \underline{\text{proved}}$$

1(b) $(A+B) \cdot (C+D)$

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$$1(b) (A+B) \cdot (C+D)$$

$$\text{Let } (A+B) = U \quad \& \quad (C+D) = V$$

then above function can be written as

$$(A+B) \cdot (C+D) = U \cdot V$$
$$= \overline{U \cdot V}$$

$$[\text{As } \overline{\overline{A}} = A]$$

$$= \overline{U} + \overline{V}$$

$$[\text{As per DeMorgan's Theorem}]$$
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Now putting value of U & V above,

$$(A+B) \cdot (C+D) = \overline{(A+B)} + \overline{(C+D)}$$

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(a) The LHS of 1(a) can be realized using two 2-input AND gates followed by one 2-input OR gate, while the RHS can be realized by two 2-input NAND gates followed by another 2-input NAND gate. Hence an AND-OR configuration is equivalent to a NAND-NAND configuration. Also, AND-OR and NAND-NAND configuration both are two level configuration.

(b) The LHS of 1(b) can be realized using two 2-input OR gates followed by one 2-input AND gate, while the RHS can be realized by two 2-input NAND gates followed by another 2-input NAND gate.

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(b) The LHS of 1(b) can be realized using two 2-input OR gates followed by one 2-input AND gate, while the RHS can be realized by two 2-input NOR gates followed by another 2-input NOR gate. Hence an OR-AND configuration is equivalent to a NOR-NOR configuration. Also OR-AND and NOR-NOR configuration both are two level configuration.

Q2) Realize the logic equation using EX-OR gates:

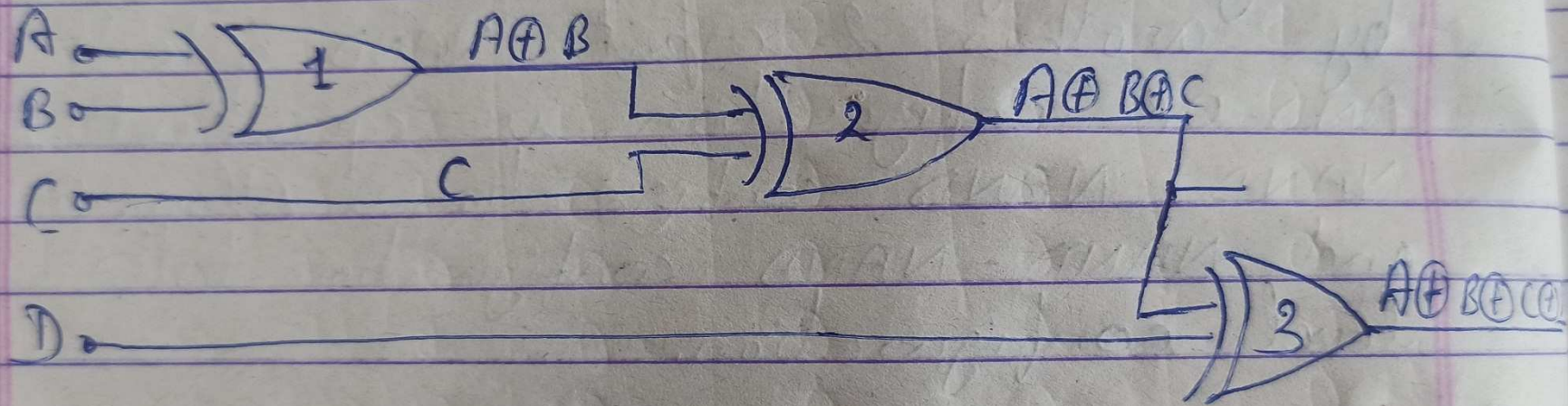
$$Y = A \oplus B \oplus C \oplus D$$

Soln: The logic function $Y = A \oplus B \oplus C \oplus D$ can be realized using EX-OR gate with ~~two~~ 2 nos. of input, or 3 nos. of input plus 2 nos. of input or 4 nos. of input. ~~EX-OR gate.~~

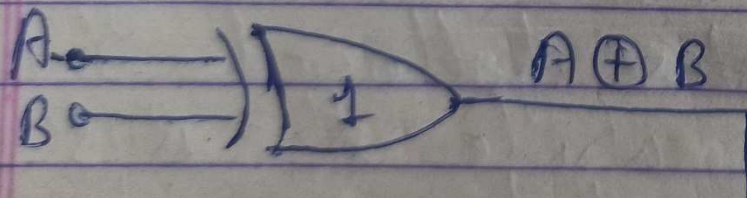
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Realization using 3 two-input EX-OR gate

$$Y = A \oplus B \oplus C \oplus D$$

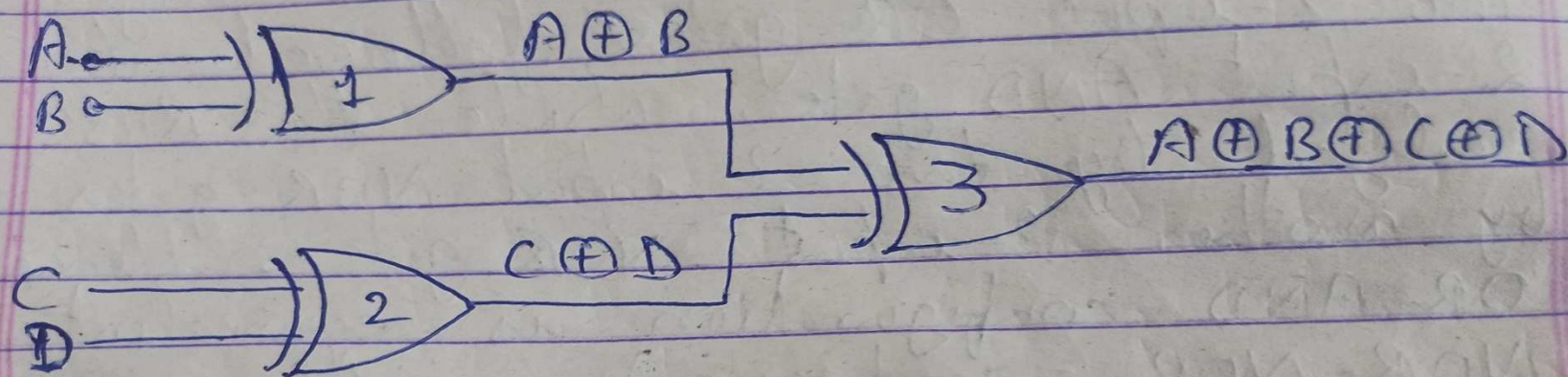


Alternative realization using 3 two-input EX-OR gate

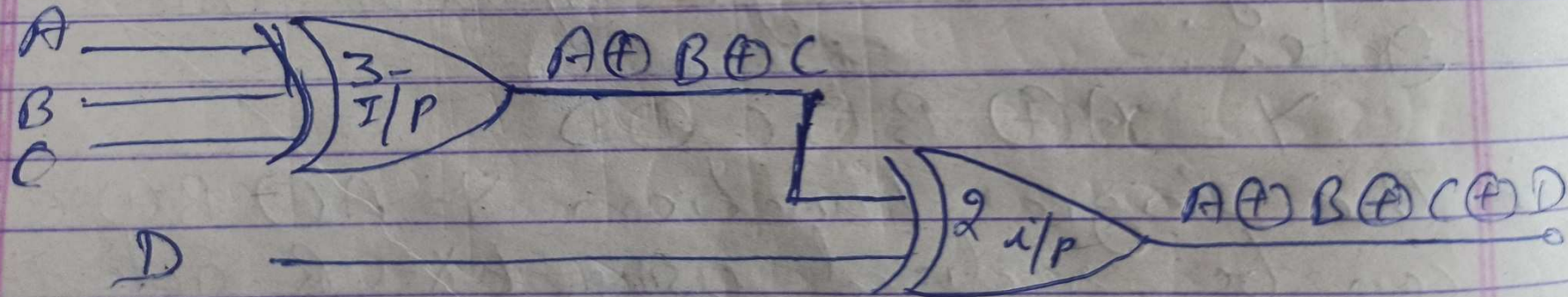


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Alternative realization

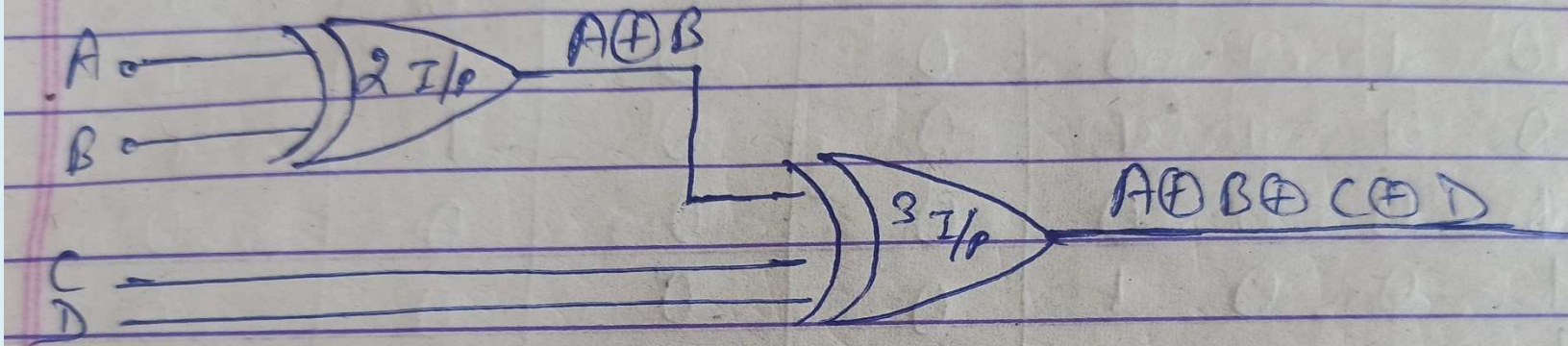


Realization using 1 three-input & 1 two-input XOR gate.

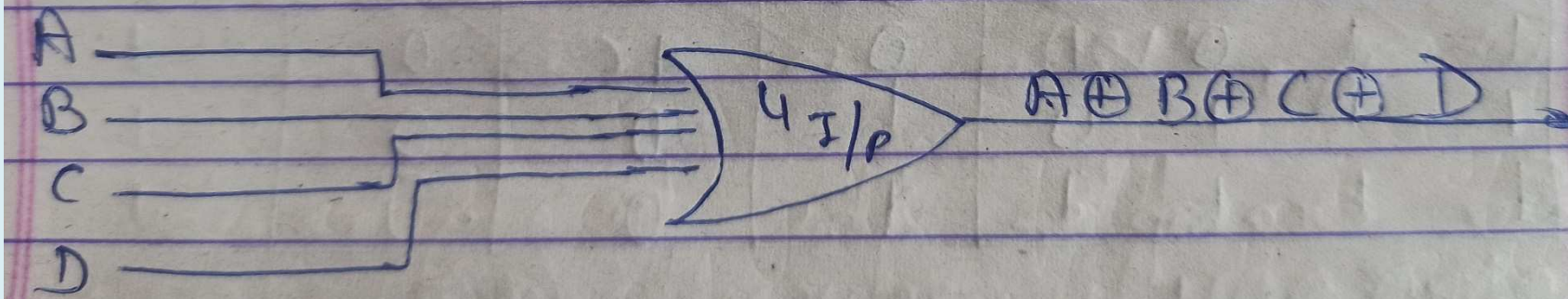


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Alternate realization using 1 three-input and 1 two-input EX-OR gate.



Realization using 1 four-input EX-OR gate.



Combinational Logic Design

Refer book- Modern Digital Electronics by RP Jain.

Thank You