

Paper 7, TDC Part-3
Chapter– 4, Combinational Logic Design
Lecture - 18

By:

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Combinational Logic Design

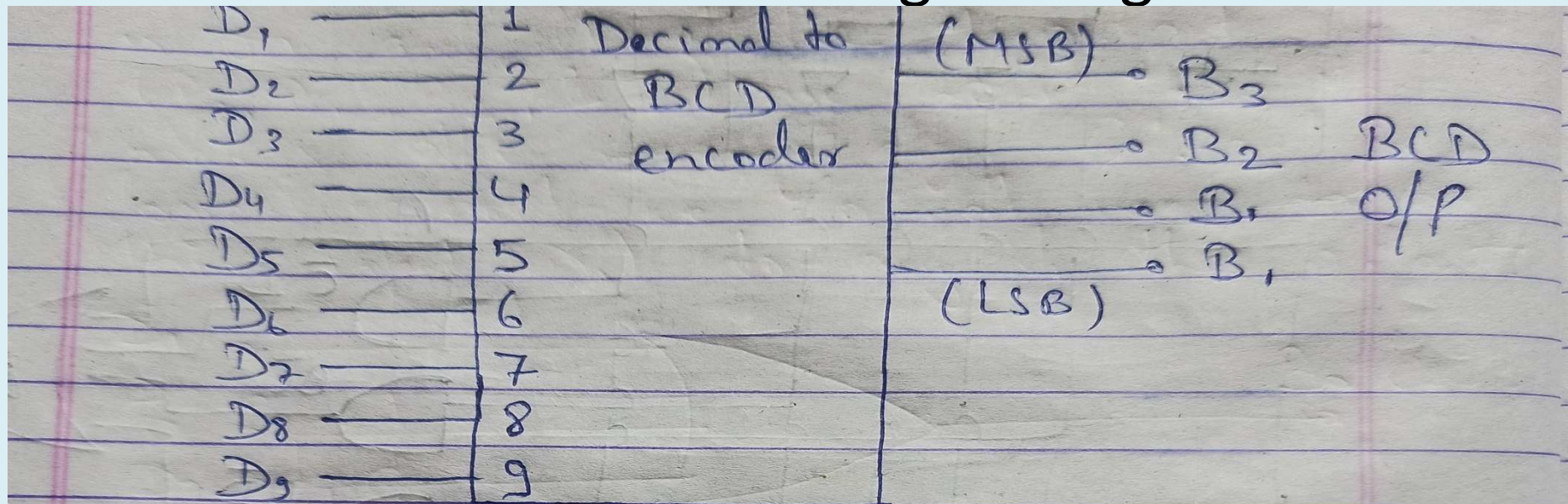
Encoder

An Encoder is a logic circuit which converts digits/symbols to a binary coded format. This process is known as encoding. It has n inputs and m outputs.

For example a decimal-to-BCD encoder has 10 inputs and 4 outputs. Each input is for each decimal digit, and the 4 outputs corresponds to BCD code of each decimal digit.

D_0	0	Decimal to BCD	(MSB) B_3
D_1	1		
D_2	2		

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Block diagram of Decimal-to-BCD encoder.

To draw the logical circuit of the ~~above~~ encoder given here we need to obtain logical expression for the output and the logical expression can be obtain from the truth table

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So we will make truth table for Decimal to BCD Encoder.

Input Decimal Digit	B_3	B_2	B_1	B_0
D_0	0	0	0	0
D_1	0	0	0	1
D_2	0	0	1	0
D_3	0	0	1	1
D_4	0	1	0	0
D_5	0	1	0	1
D_6	0	1	1	0
D_7	0	1	1	1
D_8	1	0	0	0
D_9	1	0	0	1

Truth table of Decimal-to-BCD Encoder

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From the above truth we can now write the logical expression for the outputs,

$$B_0 = D_1 + D_3 + D_5 + D_7 + D_9$$

From the truth table we can observe that output line B_0 is "high (On)" for the input line D_1, D_3, D_5, D_7, D_9 so we ~~take~~ ^{will} use 'OR' gate so that B_0 is On if either of D_1 or D_3 or D_5 or D_7 or D_9 is available at input line.

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Similarly we can write the the logical expression for other output lines too,

$$B_1 = D_2 + D_3 + D_6 + D_7$$

$$B_2 = D_4 + D_5 + D_6 + D_7$$

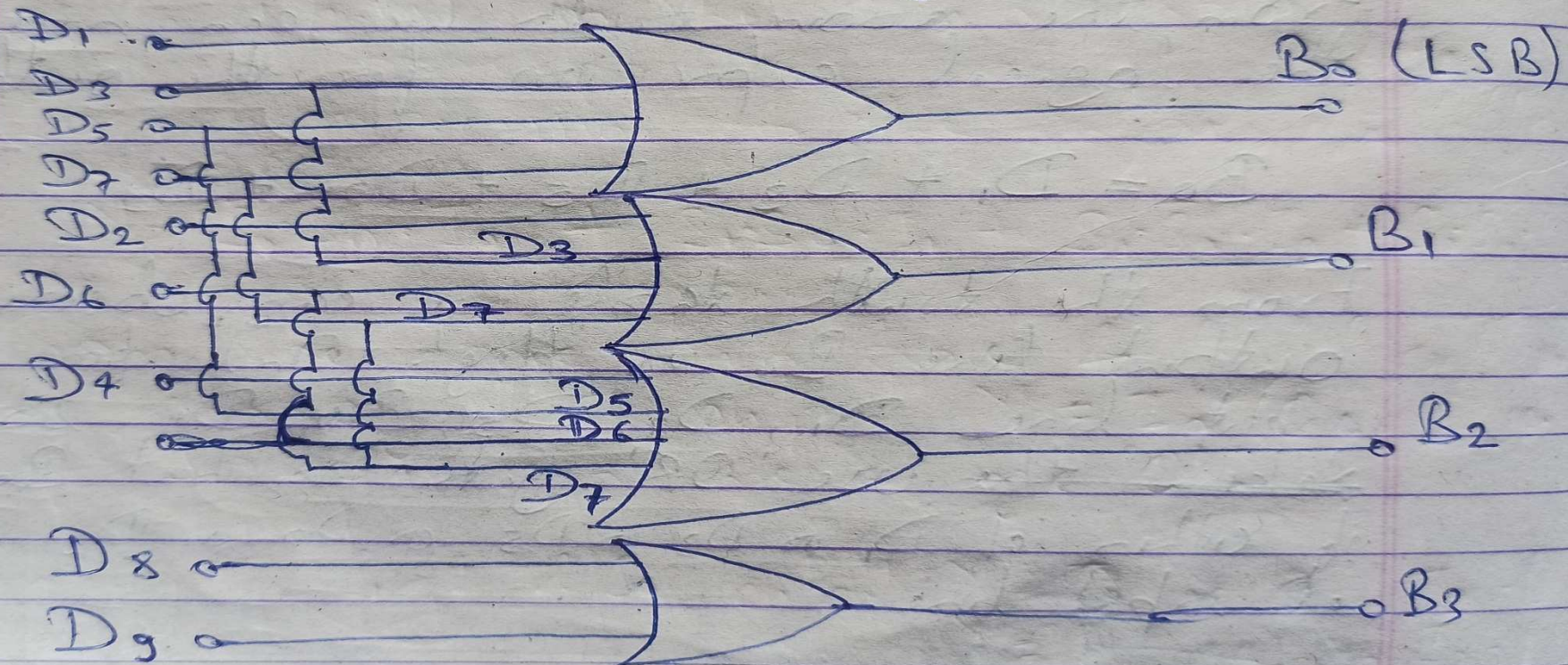
△

$$B_3 = D_8 + D_9$$

From the above expressions for 4 output lines we can see that none of the expressions include input line 'Do' i.e. if the Encoder is on and all of the "4" output lines

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is on and all the other inputs (B₀, B₁, B₂, & B₃) are "Low" then that means the binary digit '0'. and so in logical circuit we do not need to connect this input (D₀) to any of the output.

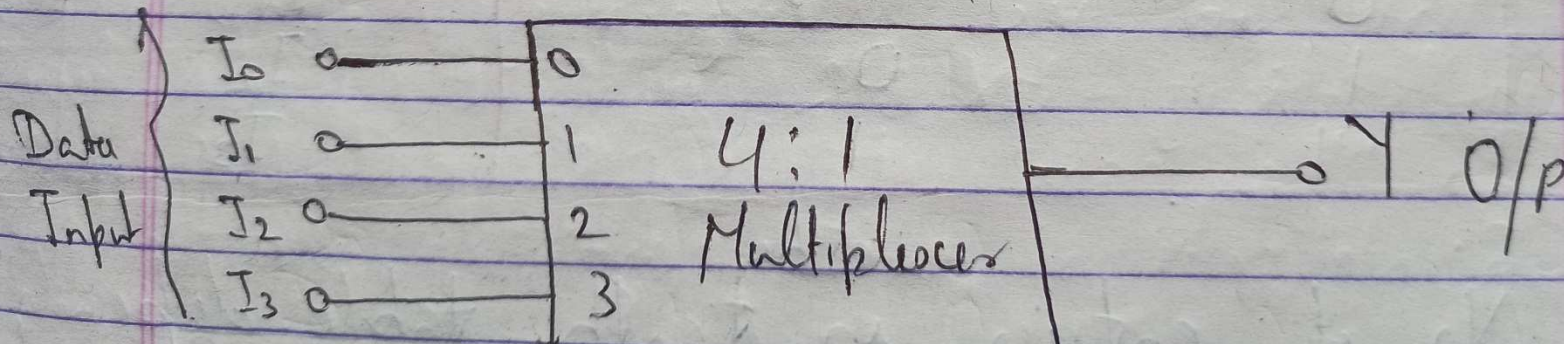


Implementation of Decimal to BCD encoder

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Multiplexer \rightarrow The multiplexer is a logic circuit that allows one of the n data inputs at the output depending on the input condition on select line. A multiplexer has two types of input one is data input and other is select input and there is only one output line.

Figure below shows the block diagram of a 4:1 multiplexer



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single Output.

When a multiplexer is On, one of the data Inputs will appear at output depending on the value of select line. The truth table for a 4:1 multiplexer is given below

Select Input		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

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So No. of entries in ^{the} truth table depends on the number of select lines. For 2 select line there will be 4 entries (as well as 4 data inputs) in the truth table.

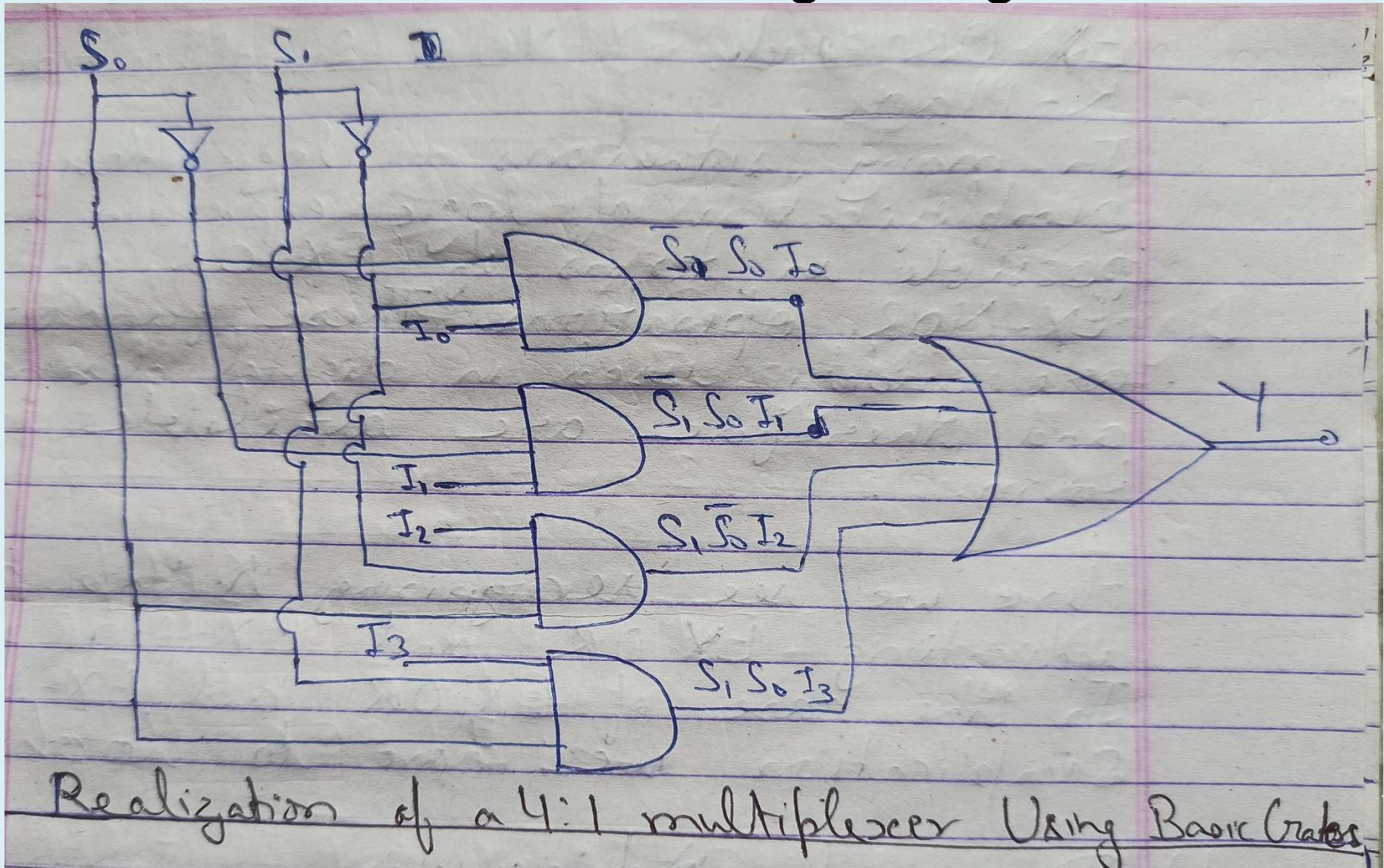
Logical expression for the output of a Multiplexer ^{4:1}

$$Y = \bar{S}_1 \cdot \bar{S}_0 \cdot I_0 + \bar{S}_1 \cdot S_0 \cdot I_1 + S_1 \cdot \bar{S}_0 \cdot I_2 + S_1 \cdot S_0 \cdot I_3$$

From the above truth table & logical expression we can say that output $Y = I_0$ (0 or 1) i.e. if S_1 & S_0 both are at logic '0'.

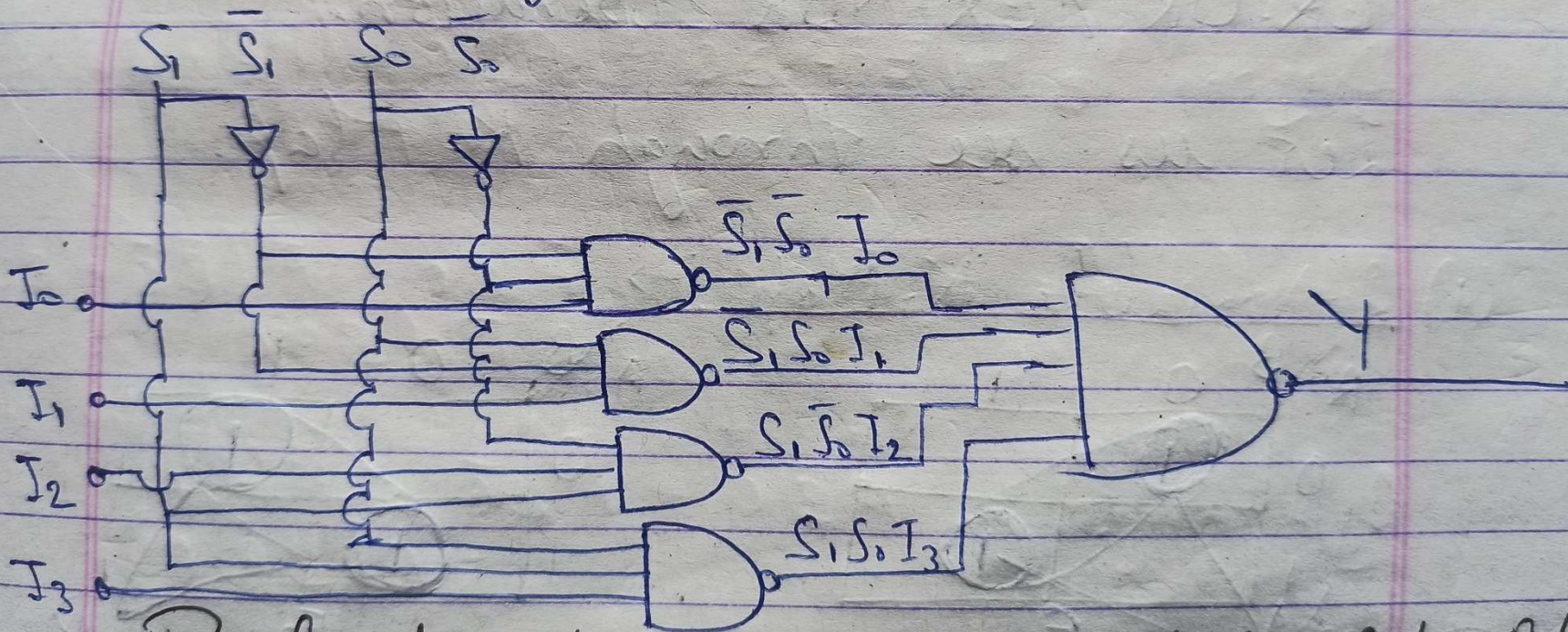
Similarly if $S_1 = 1$ & S_0 output $Y = I_2$ i.e. if $I_2 = 0$
 $Y = 1$ i.e. if $I_2 = 1$

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Since the o/p Y of multiplexer has obtained in SOP form so we can also implement the multiplexer logic circuit using NAND gates easily.



Realization of 4:1 Mux using NAND Gates Only.

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Refer book- Modern Digital Electronics by RP Jain.

Thank You