Paper 7, TDC Part-3
Chapter– 4, Combinational Logic Design
Lecture - 14

By:

Mayank Mausam

Assistant Professor (Guest Faculty)

Department of Electronics

L.S. College, BRA Bihar University,

Muzaffarpur, Bihar

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3. Half-Subtractor :- A logic ckt. for the subtraction of B (subtrahend) from A (minuend) is referred to as a half-subtractor, here A & B are 1-bit numbers.

Rules of Binary Subtraction is just like decimal ~~subtraction~~ number subtraction process and is illustrated in below truth table

Minuend (A)	Subtrahend (B)	Difference (D)	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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In a subtraction process of two binary numbers is as below.

→ If the minuend and subtrahend both are equal then difference & borrow both will be '0'.

→ When the minuend is greater than subtrahend then the difference is '1' while borrow is '0'.

→ When the minuend is smaller than subtrahend then the minuend will borrow 1 from the higher bit of minuend, then the minuend will become greater than the

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subtrahend and the subtraction will result as difference = 1 & borrow = 1.

As per truth table the difference part for 4 different conditions for a two 1 bit number can be implemented with Ex-OR gate while the borrow part can be realized using "NOT" gate & "AND" gate.

i.e. $D = \bar{A}B + A\bar{B} = A \oplus B$

$B_w = \bar{A}B$

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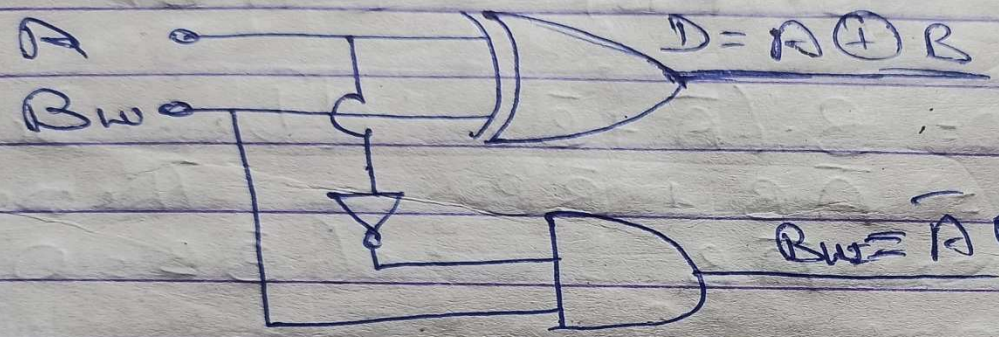
Realization of Half Subtractor using gates is shown below:->



* Realization of Half subtractor ckt using NAND gates only.

As we have seen that the half subtractor can be realized using Ex-OR gate, AND gate and NOT gate.

In the half-adder section we have realized the Ex-OR gate using 4-NAND gates only.

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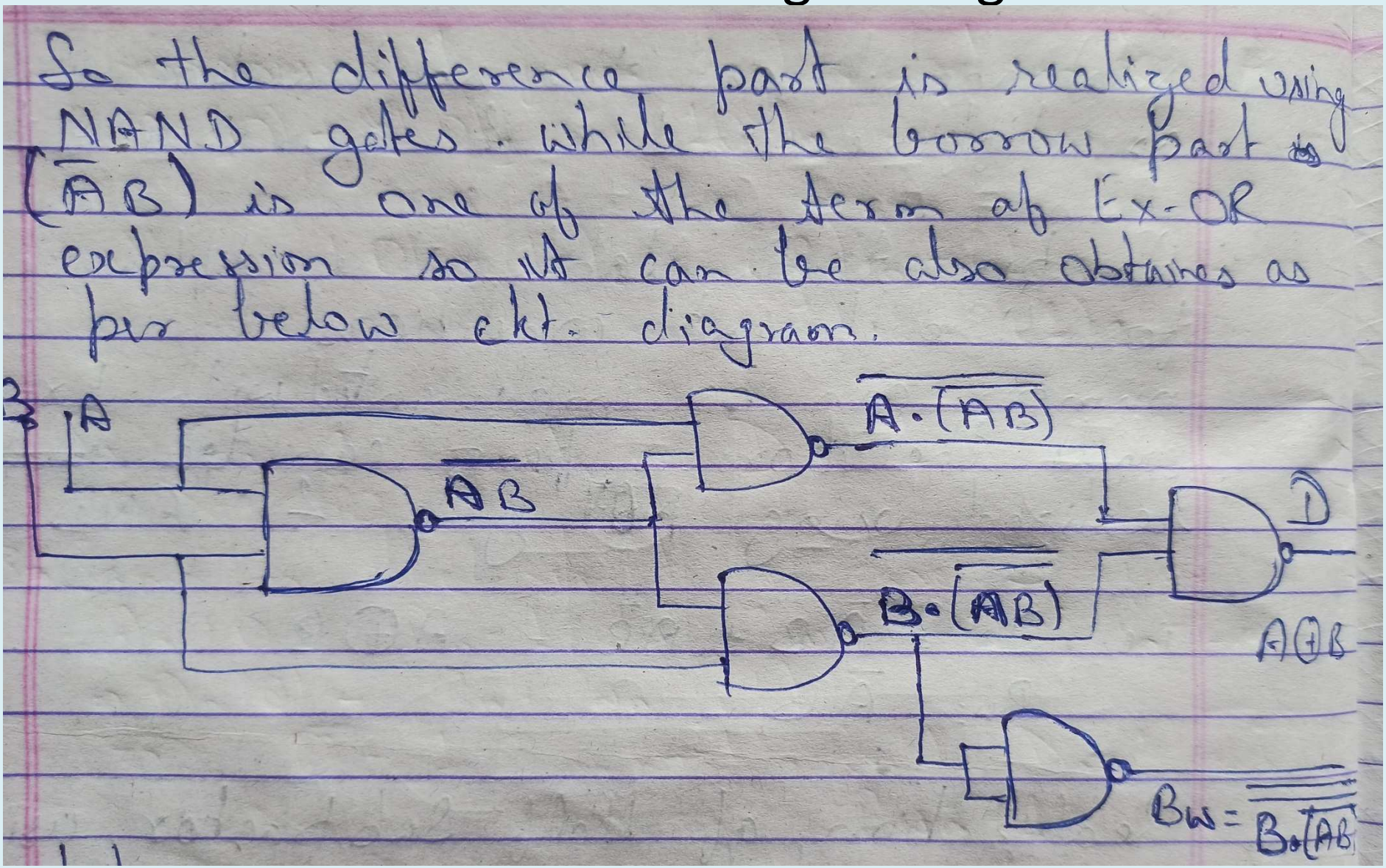

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Let us see :-

$B_W = B \cdot (\overline{AB}) = B \cdot (\overline{A} + \overline{B})$ [Using De Morgan's Theorem]

$= B \cdot (\overline{A} + \overline{B})$

$= \overline{A}B + \overline{B}B$ [$\overline{B}B = 0$]

$B_W = \overline{A}B$

also

So a half subtractor ckt can be realized using 5 NAND gates only. like a half adder ckt.

Full Subtractor :-> For performing subtraction of two multibit numbers we need as many full subtractor block ckt as there are bits in the number. A full subtractor ckt includes three inputs

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A_n (minuend), B_n (subtrahend) and $B_{W_{n-1}}$ (borrow from the previous stage and two outputs, D_n (difference) and B_{W_n} (borrow). The truth table for a full subtractor is given below.

Inputs			Outputs	
A_n	B_n	$B_{W_{n-1}}$	D_n	B_{W_n}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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Refer book- Modern Digital Electronics by RP Jain.

Thank You