

Paper 7, TDC Part-3
Chapter– 4, Combinational Logic Design
Lecture - 13

By:

Mayank Mausam

Assistant Professor (Guest Faculty)

Department of Electronics

L.S. College, BRA Bihar University,

Muzaffarpur, Bihar

Combinational Logic Design

① ~~NAND-NAND realization of half adder & full adder~~

In a half adder and full adder we have two o/p's, one is sum part & other is carry part.

~~NAND-NAND realization of Half-Adder~~

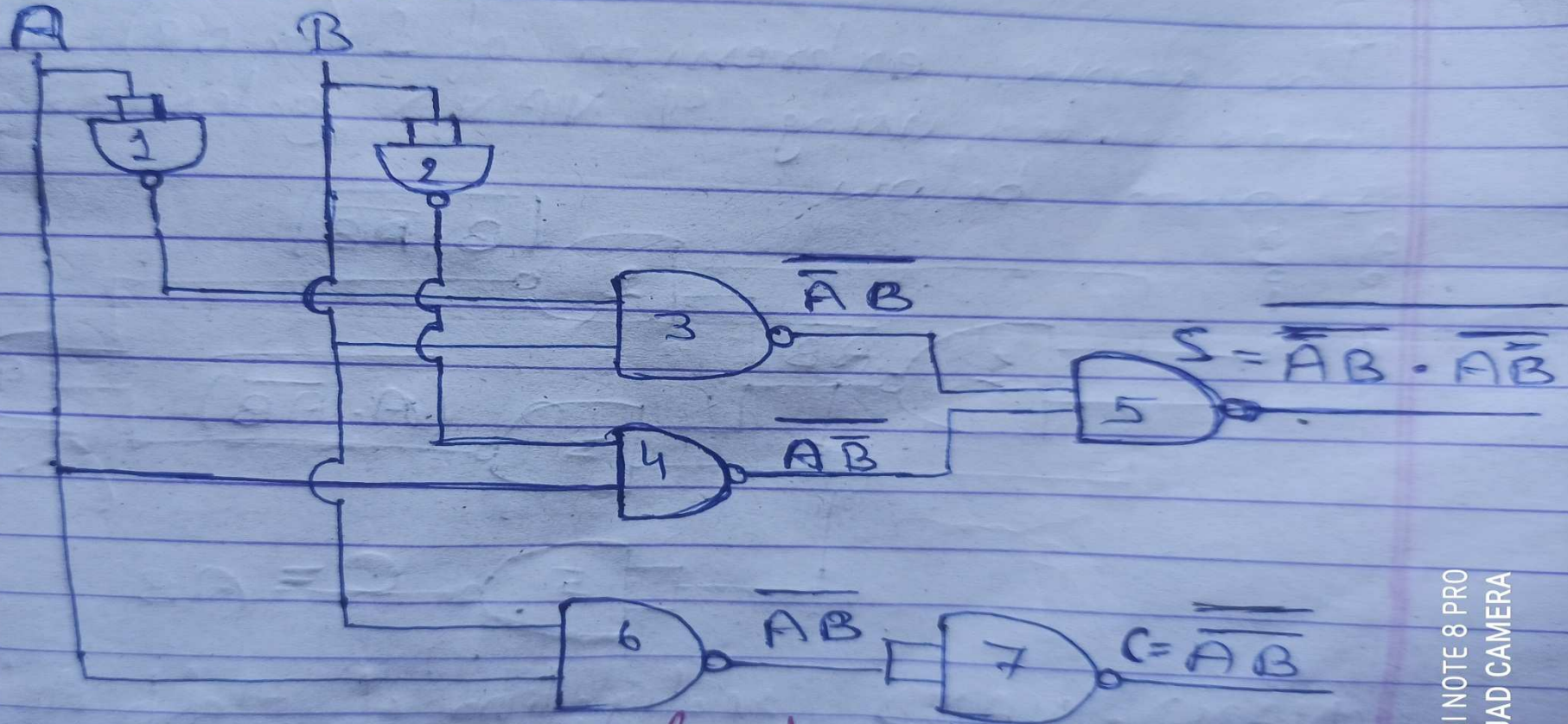
For Half Adder \Rightarrow

$$S = \bar{A}B + A\bar{B} \quad \therefore \quad \overline{\overline{\bar{A}B + A\bar{B}}}$$

$$= \overline{\overline{\bar{A}B} \cdot \overline{A\bar{B}}} = \overline{\overline{\bar{A}B}} \cdot \overline{\overline{A\bar{B}}}$$

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$$C = AB = \overline{\overline{AB}}$$



NAND-NAND realization of half adder using 7 NAND gates

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We can also implement Sumparast (i.e. expression $\bar{A}B + A\bar{B}$ which is nothing but Ex-OR function) using 4 ^{NAND} gates only, as below:-

$$S = \bar{A}B + A\bar{B} = (A+B)(\bar{A}+\bar{B}) \quad \text{Using Transposition theorem}$$

$$S = \overline{\overline{(A+B)(\bar{A}+\bar{B})}} = \overline{\overline{(A+B)} \cdot \overline{\overline{(\bar{A}+\bar{B})}}}$$

$$= \overline{(A+B) \cdot \overline{AB}}$$

[Using De Morgan's Theorem]

$$= \overline{A \cdot \overline{AB} + B \cdot \overline{AB}}$$

$$= \overline{(A \cdot \overline{AB}) + (B \cdot \overline{AB})}$$

[Again Using De Morgan's Theorem]

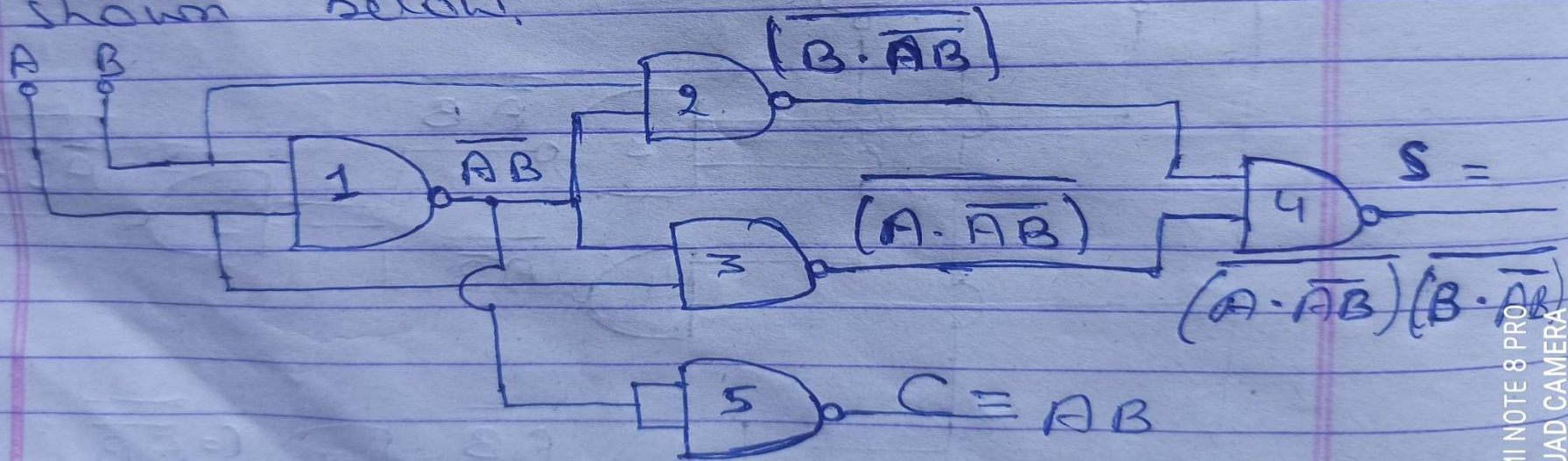
$$S = \overline{(A \cdot \overline{AB})} \cdot \overline{(B \cdot \overline{AB})}$$

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$$= (A \cdot \overline{AB}) + (B \cdot \overline{AB}) \quad (\text{Again using De Morgan's Theorem})$$

$$S = \overline{(A \cdot \overline{AB}) (B \cdot \overline{AB})}$$

The above expression of S (Ex-OR) can be implemented using 4 NAND gates only as shown below.



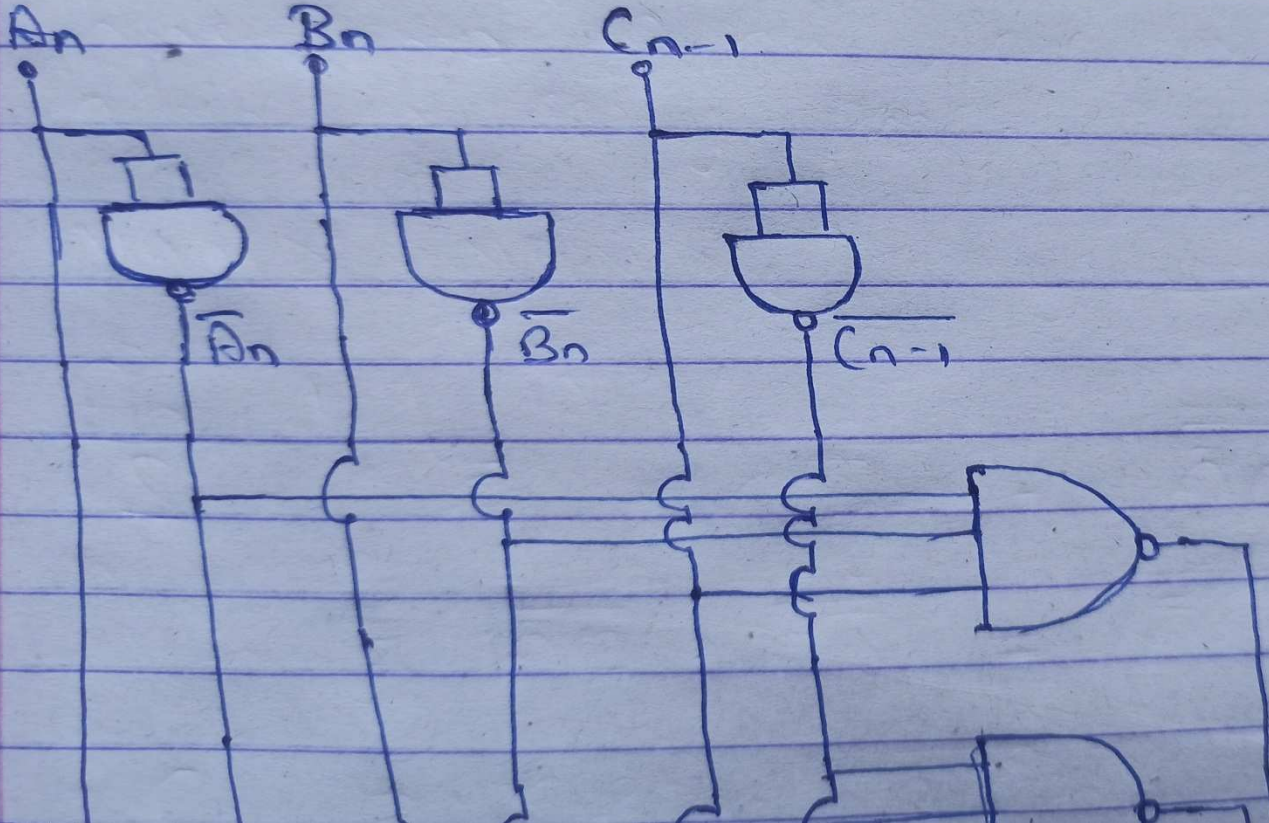
NAND-NAND realization of Half Adder using 5 NAND gates only.

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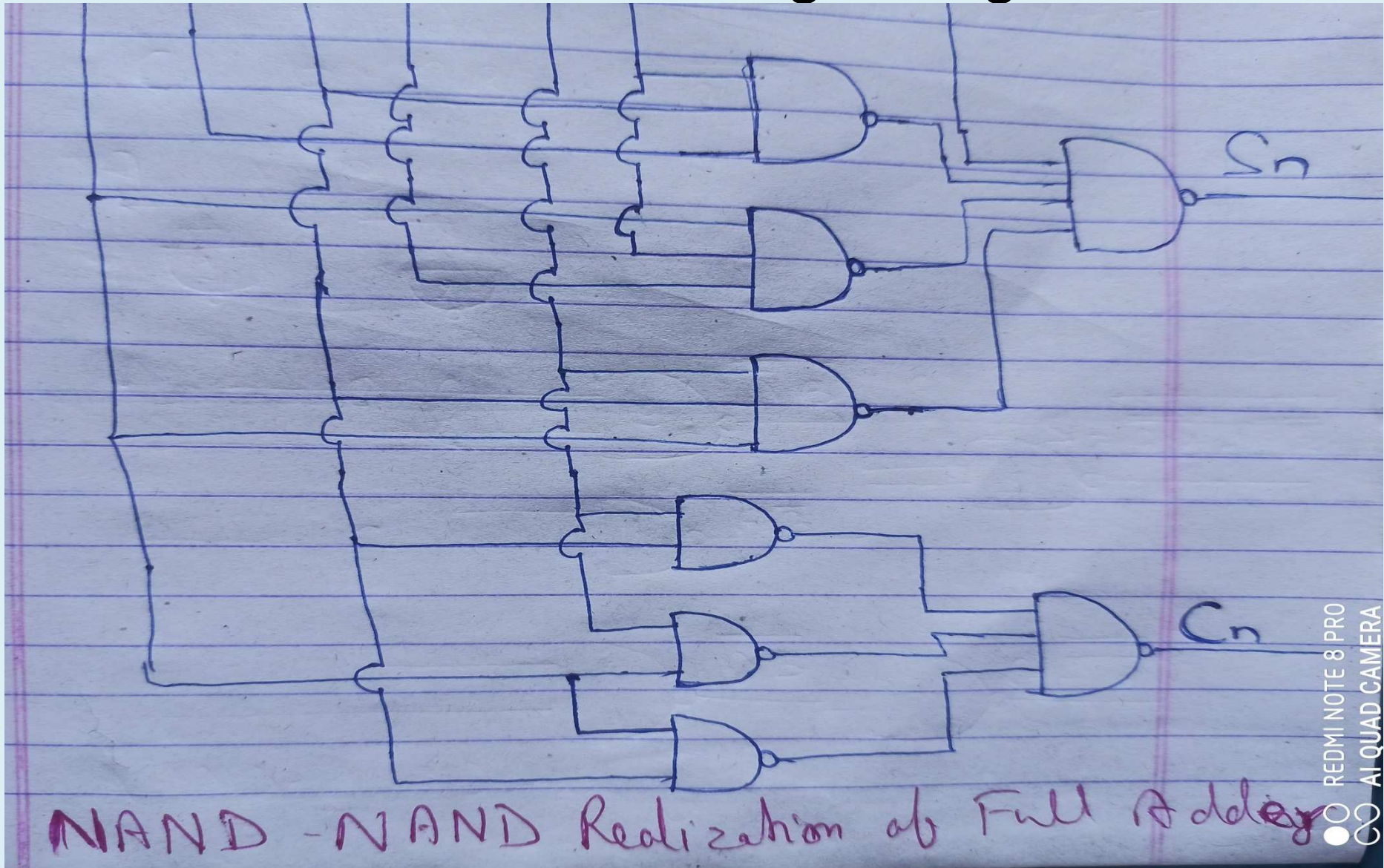
NAND-NAND realization of Full Adder ckt.

For full-adder: \rightarrow

$$S_n = \bar{A}_n \bar{B}_n C_{n-1} + \bar{A}_n B_n \bar{C}_{n-1} + A_n \bar{B}_n \bar{C}_{n-1} + A_n B_n C_{n-1}$$
$$C_n = B_n C_{n-1} + A_n C_{n-1} + A_n B_n$$



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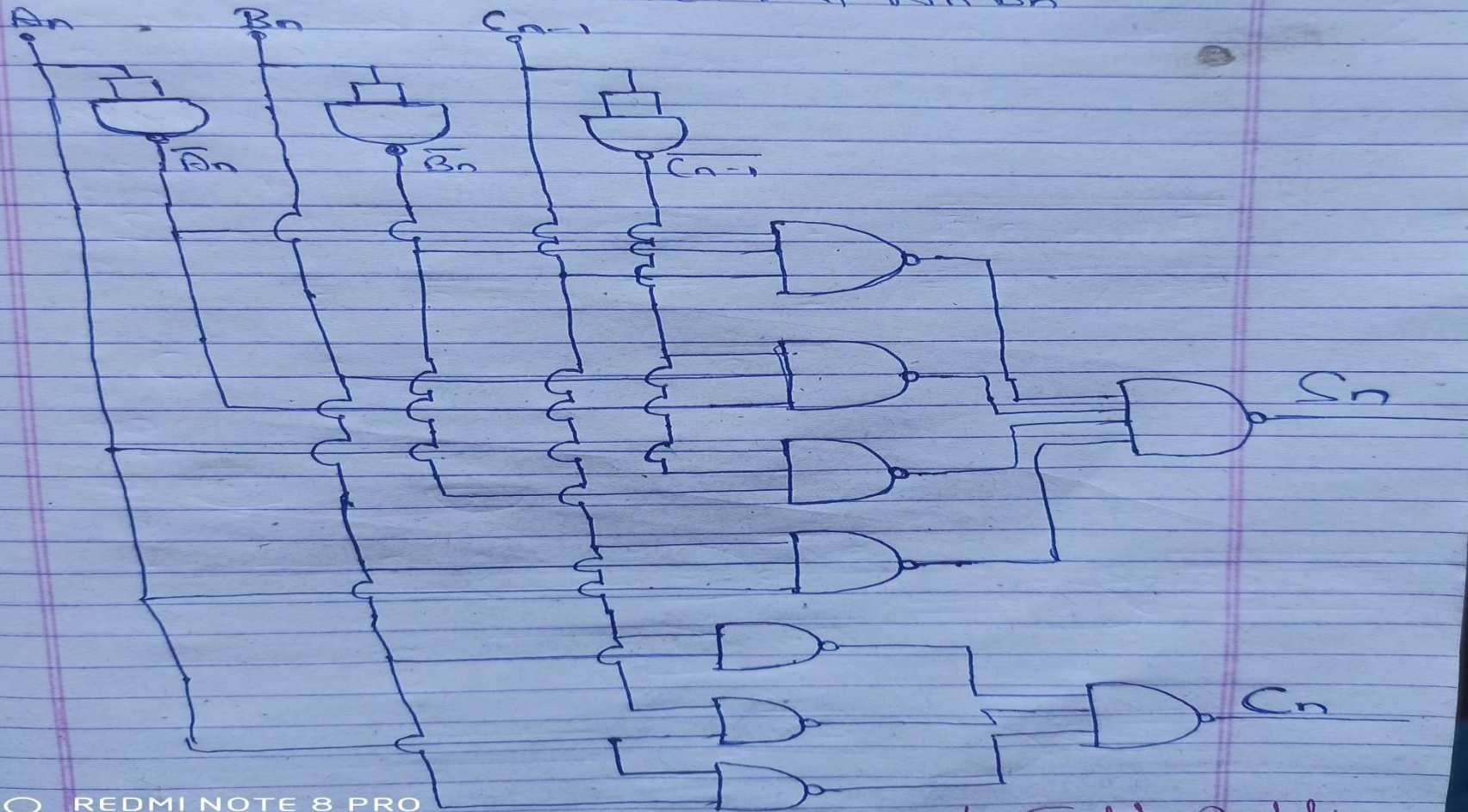


NAND - NAND Realization of Full Adder

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* NAND-NAND realization of Full Adder ckt.
For full adder \rightarrow

$$S_n = A_n B_n C_{n-1} + \overline{A_n} B_n \overline{C_{n-1}} + A_n \overline{B_n} \overline{C_{n-1}} + \overline{A_n} \overline{B_n} C_{n-1}$$
$$C_n = B_n C_{n-1} + A_n C_{n-1} + A_n B_n$$



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NAND-NAND Realization of Full Adder

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Refer book- Modern Digital Electronics by RP Jain.

Thank You