Paper 7, TDC Part-3
Chapter– 4, Combinational Logic Design
Lecture - 13

By:

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Combinational Logic Design

NAND - NAND realization of half adder & full Adder

In a half adder and full adder we have two o/p's, one is sum part & other is carry part.

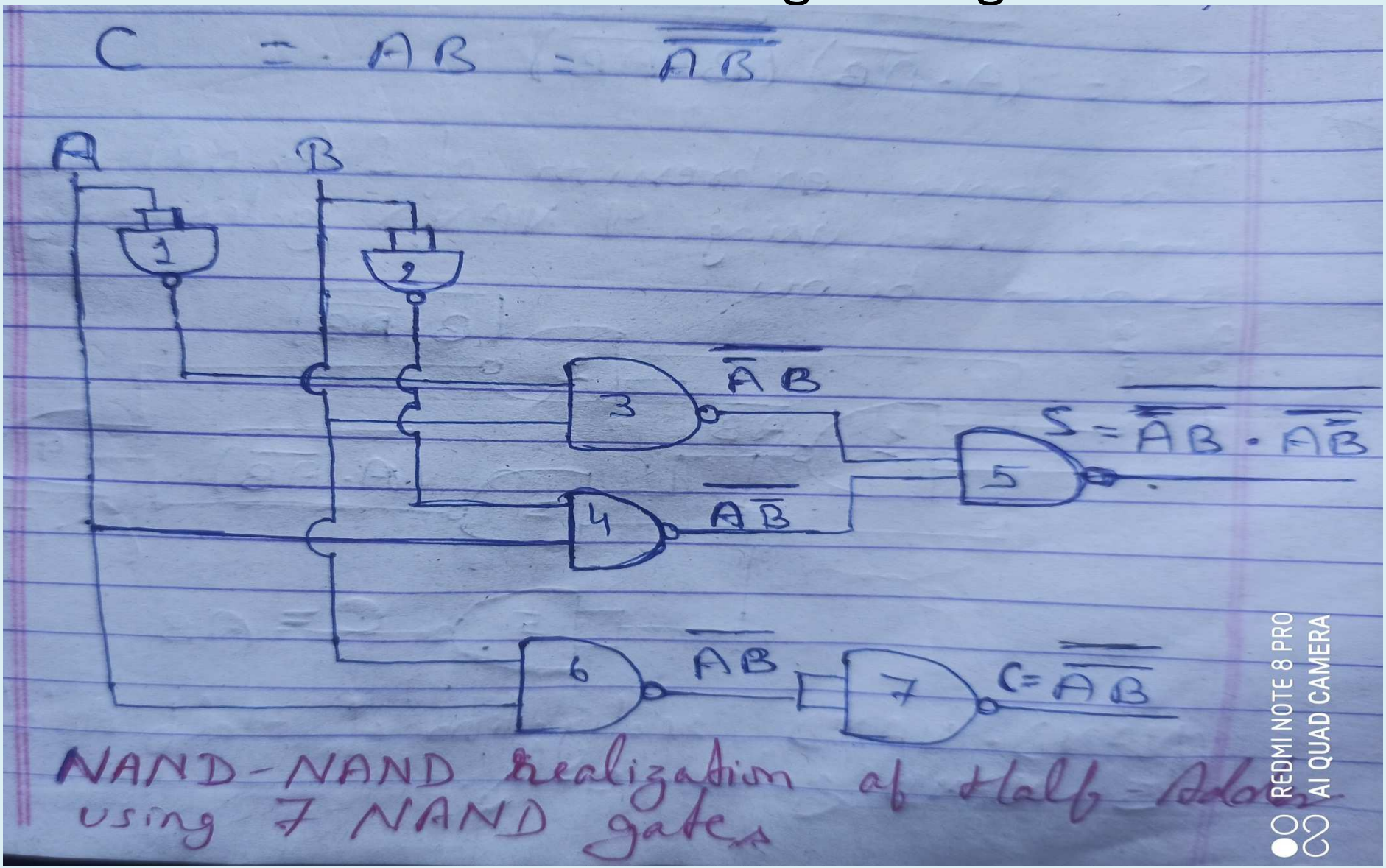
NAND - NAND realization of Half-Adder

For Half Adder :-

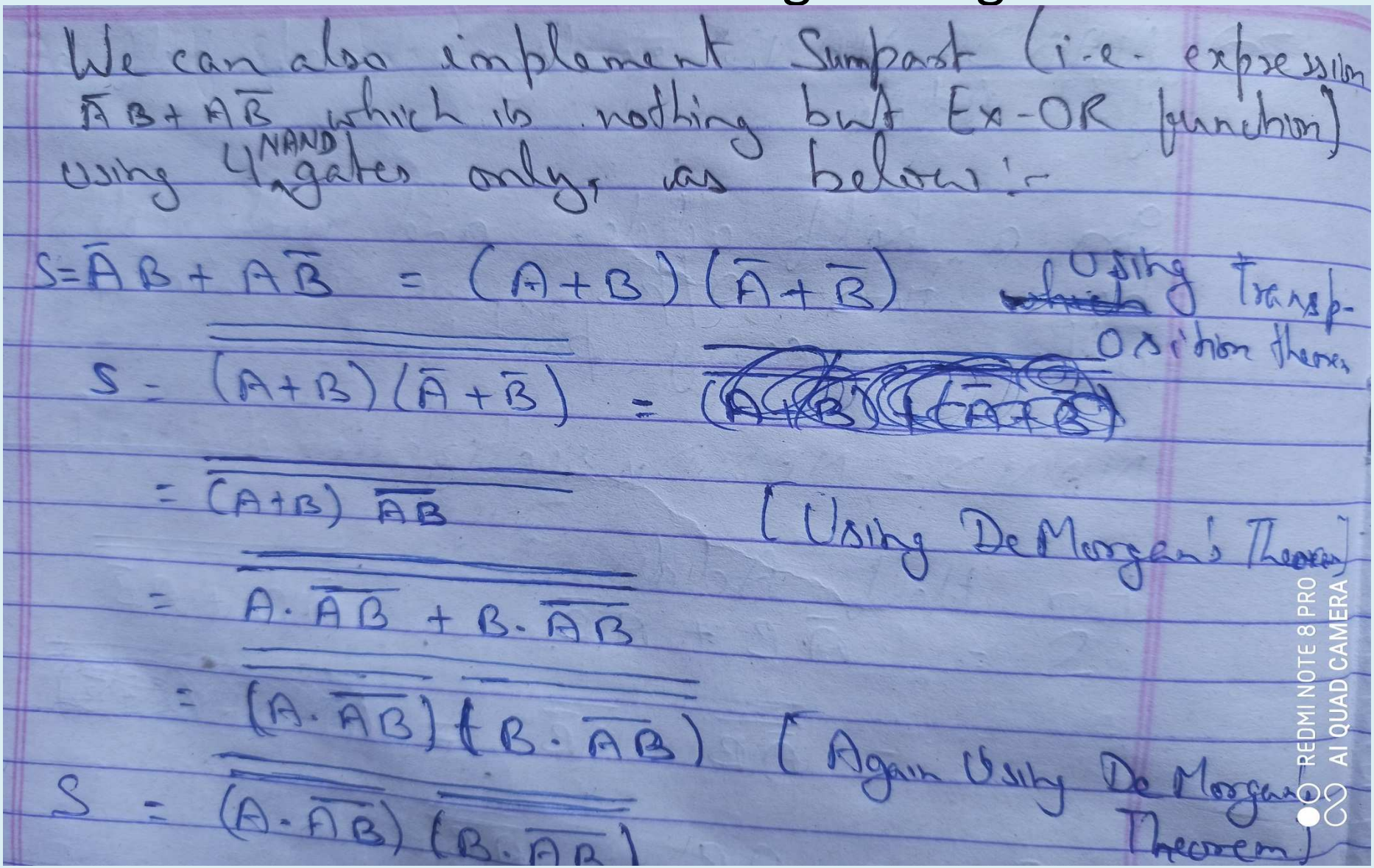
$$S = \bar{A}B + A\bar{B} = \overline{\bar{A}B + A\bar{B}}$$

$$= \overline{\bar{A}B} \cdot \overline{A\bar{B}} =$$

Combinational Logic Design



Combinational Logic Design

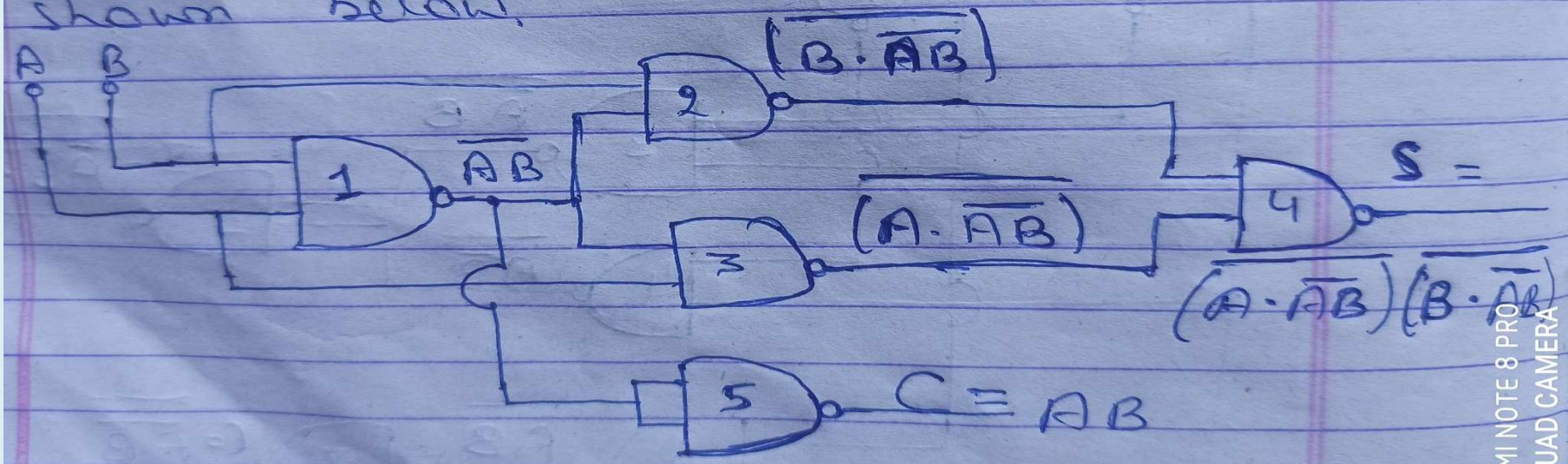


Combinational Logic Design

$= (A \cdot \overline{AB}) + (B \cdot \overline{AB})$ [Again using ... Theorem]

$S = \overline{(A \cdot \overline{AB})}\,\overline{(B \cdot \overline{AB})}$

The above expression of S (Ex-OR) can be implemented using 4 NAND gates only as shown below.



NAND-NAND realization of Half Adder using 5 NAND gates only.

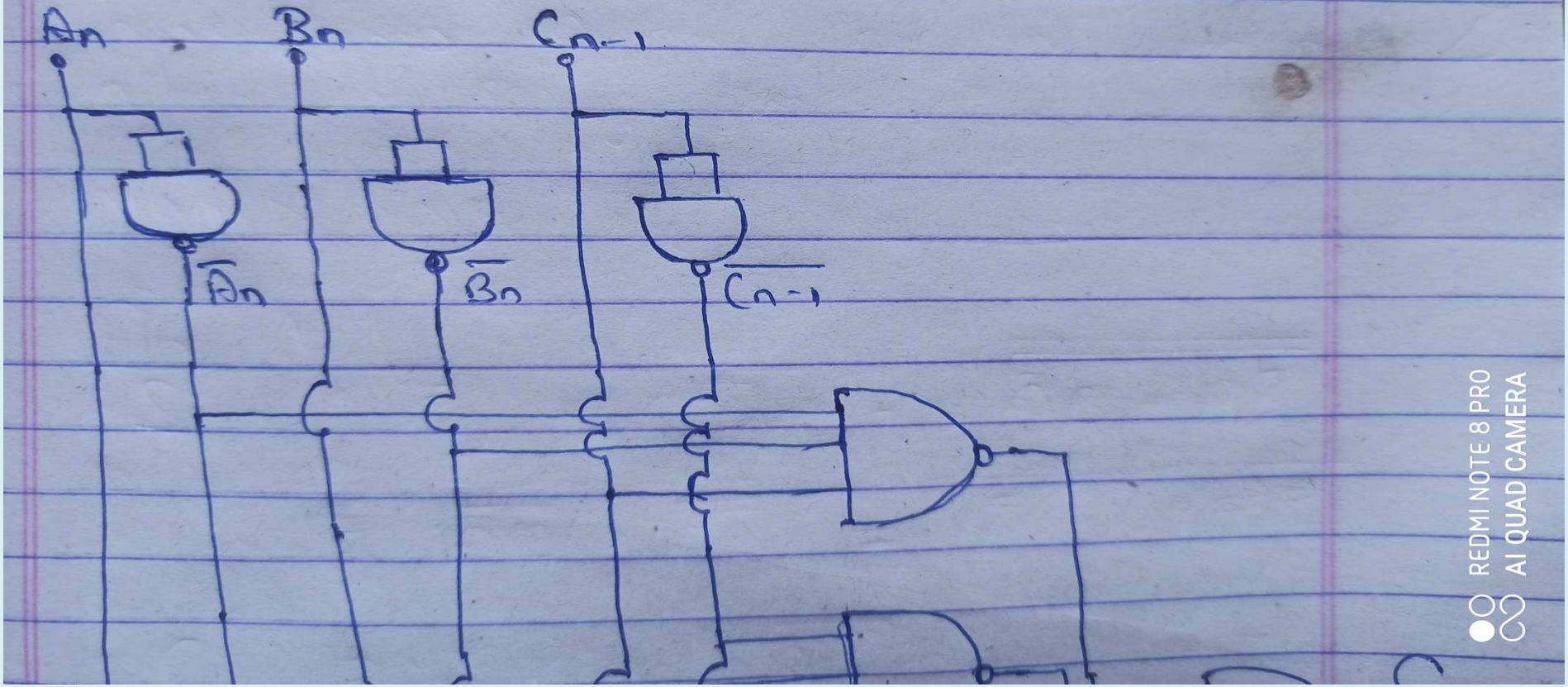
Combinational Logic Design

NAND - NAND realization of Full Adder ckt.

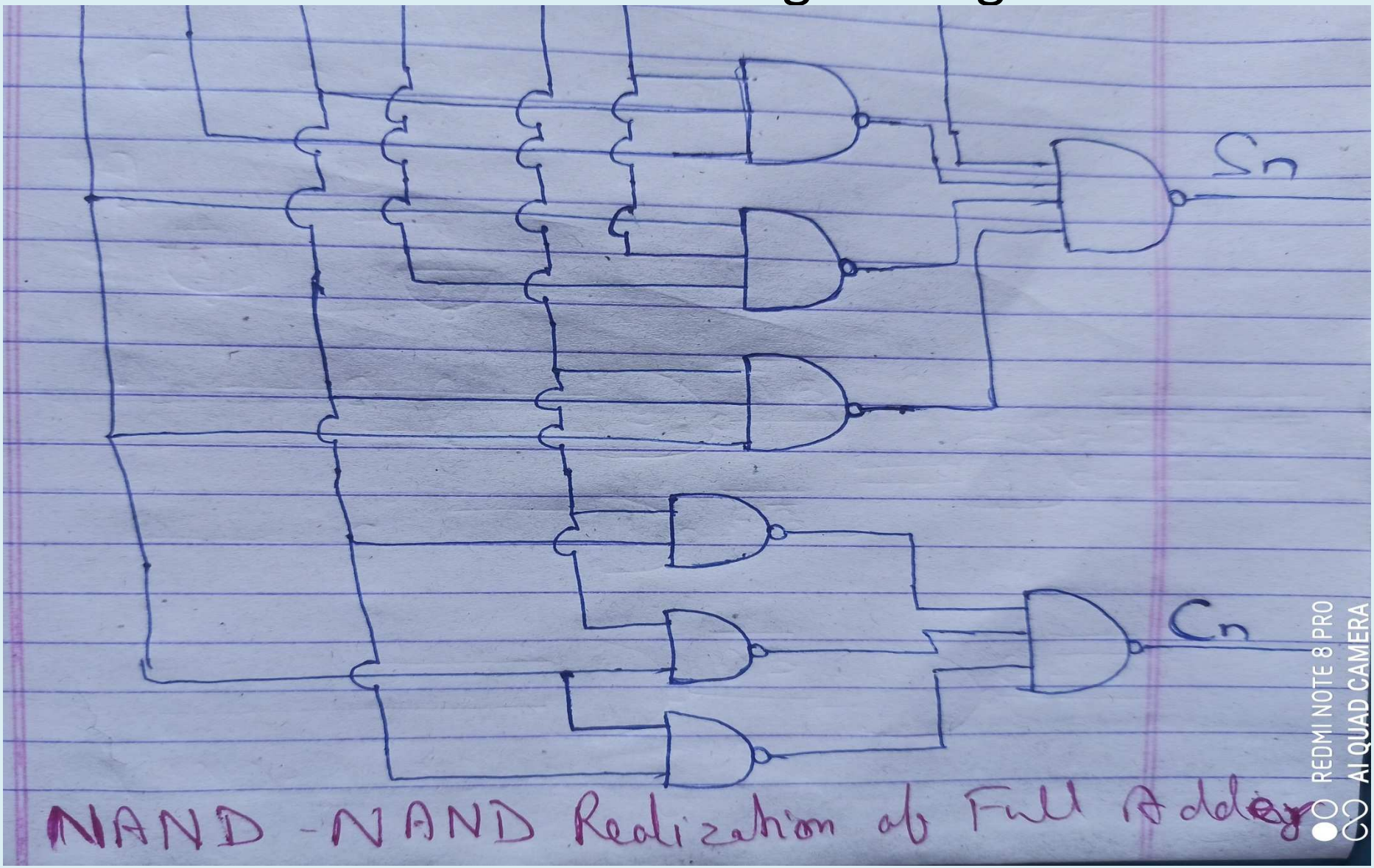
For full - adder :→

$S_n = \bar{A}_n \bar{B}_n C_{n-1} + \bar{A}_n B_n \bar{C}_{n-1} + A_n \bar{B}_n \bar{C}_{n-1} + A_n B_n C_{n-1}$

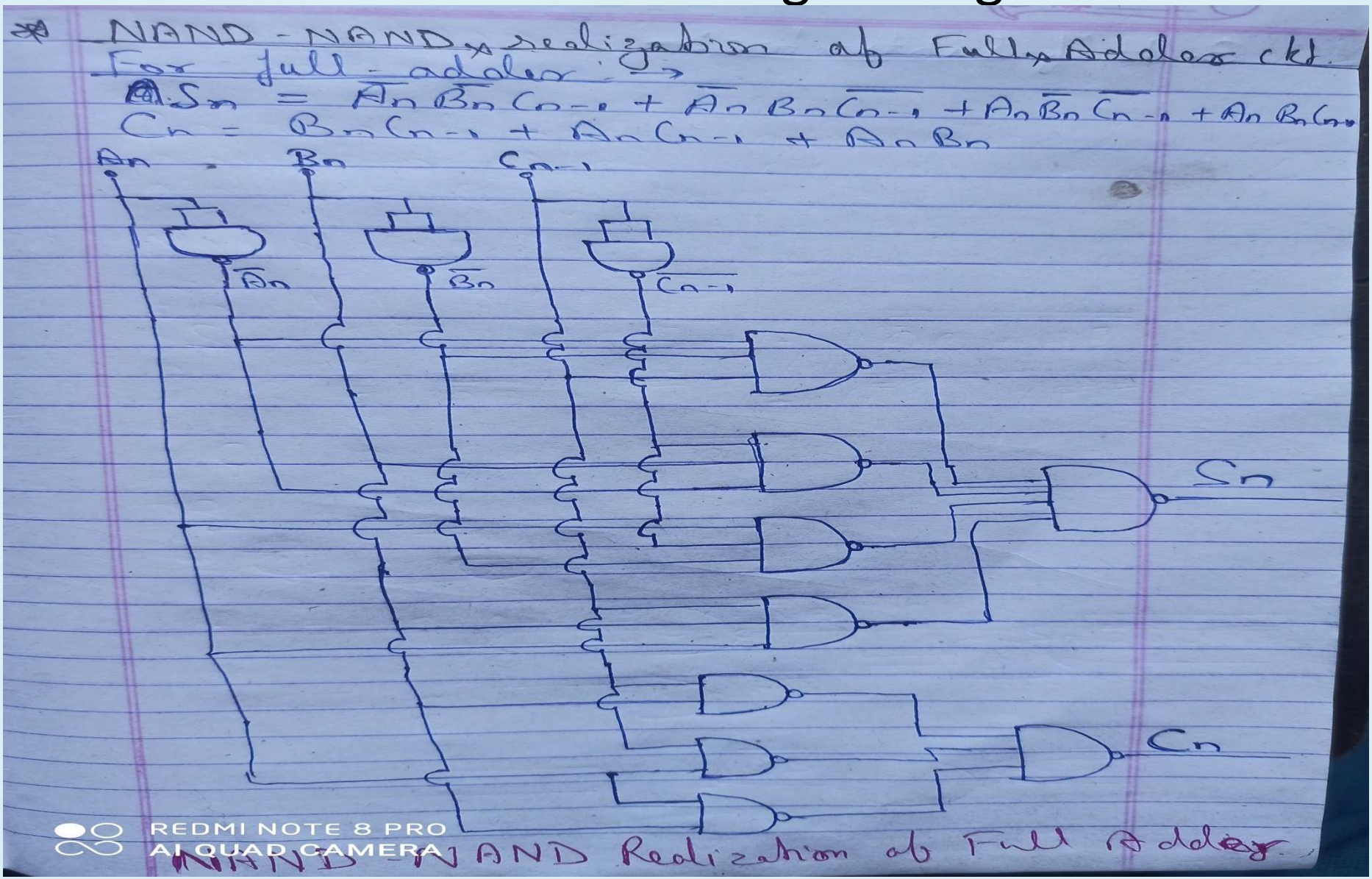
$C_n = B_n C_{n-1} + A_n C_{n-1} + A_n B_n$



Combinational Logic Design



Combinational Logic Design



Combinational Logic Design

Refer book- Modern Digital Electronics by RP Jain.

Thank You