Paper 7, TDC Part-3
Chapter– 4, Combinational Logic Design
Lecture - 12

By:

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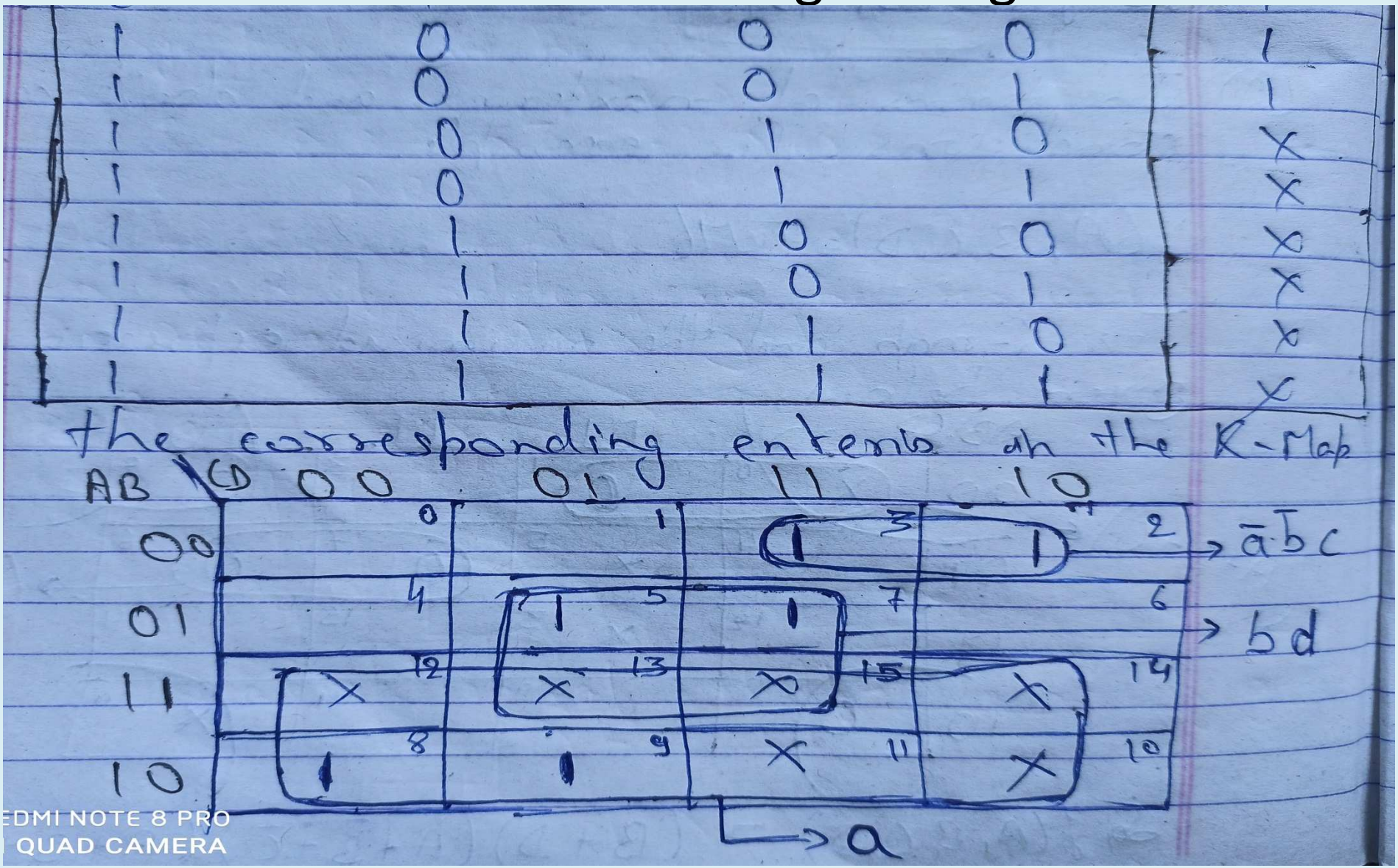
Combinational Logic Design

(3) In terms of truth table. For example, consider the truth table given below.

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1

Combinational Logic Design



Combinational Logic Design

The simplified logic function obtained from the K-Map simplification is

$$F(A, B, C, D) = a + bd + \bar{a}\bar{b}c$$

* Design Examples :-

(1) Arithmetic Circuits :- A logic circuit that perform the addition of 2 one-bit numbers is referred to as an half-adder. The output of the half adder circuit will have 2 bit, one bit is for 'Sum (S)' and the 2nd bit is for "Carry (C)". As a half adder circuit perform addition of 2-bits so it will have 2 input line.

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addition of 2-bits so it will have 2 inputs line.

Process of addition of binary bits

Augend	Addend	Sum	Carry	Result
0	0	0	0	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	10

for first 3 cases (i.e. combination of inputs) there is no carry generation. The 4th input combination produces a "carry=1".

In a half adder circuit the carry part can't

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propagate to higher binary position.

Truth Table for an Half-adder circuit

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

So from truth table we can see that sum part is obtained using "Ex-OR" gate and carry part can be obtained using "AND" gate

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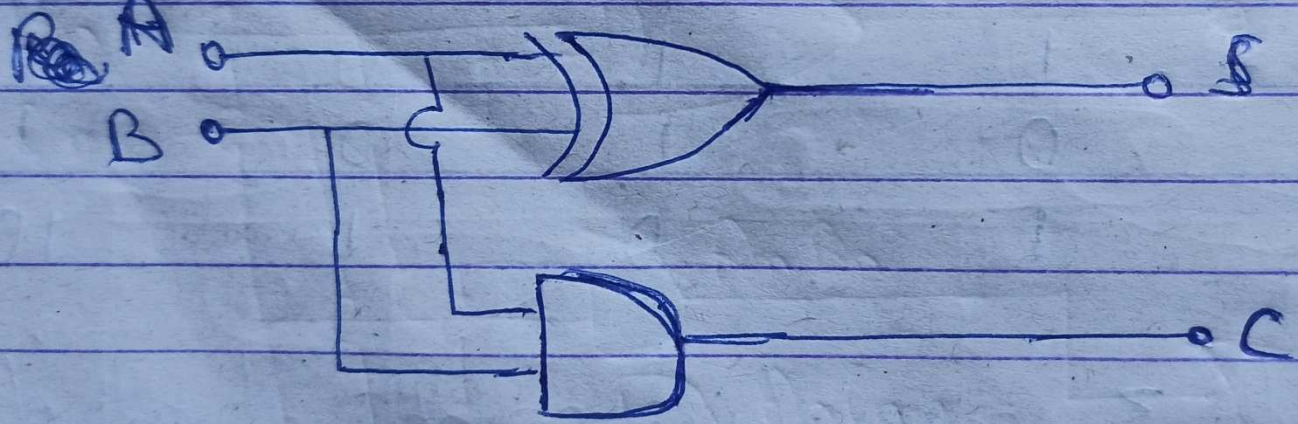
$S = \bar{A}B + A\bar{B} = A \oplus B$

$C = AB$

So a half adder can be realised using "Ex-OR and AND" gate



Realisation of Half-Adder using Gates

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respectively and C_{n-1} is the carry generated from the addition of $(n-1)$ th orders bits. This circuit is referred to as "Full-Adder". The truth table for a full-adder is given below.

Inputs			Outputs	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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We can realised the outputs 'Sn' & 'Cn' using 3-variable K-map, as shown below.

A_n \ $B_{n-1}C_{n-1}$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

K-Map for S_n

A_n \ $B_{n-1}C_{n-1}$	00	01	11	10
0	0		1	
1		1	1	1

K-Map for C_n

We can see that 0 in K-map for Sum (S_n) no groups of 1's is possible i.e. All 1's are single. so expression for S_n is given as

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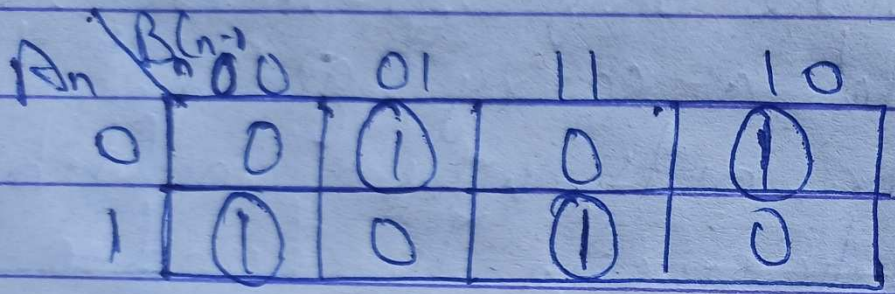
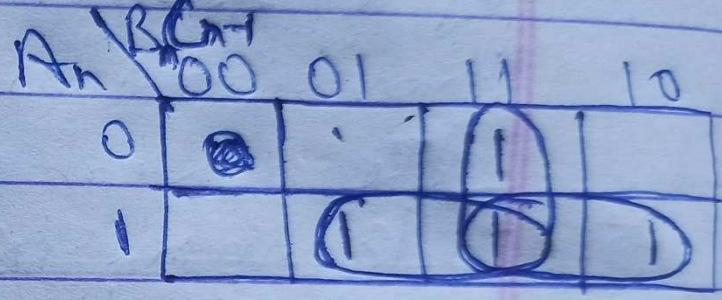
We can realised the outputs 'Sn' & 'Cn' using 3-variable K-map, as shown below



K-Map for Sn



K-Map for Cn

We can see that 0 in K-map for Sum (Sn) no groups of 1's is possible i.e. all 1's are single. so expression for Sn is given as

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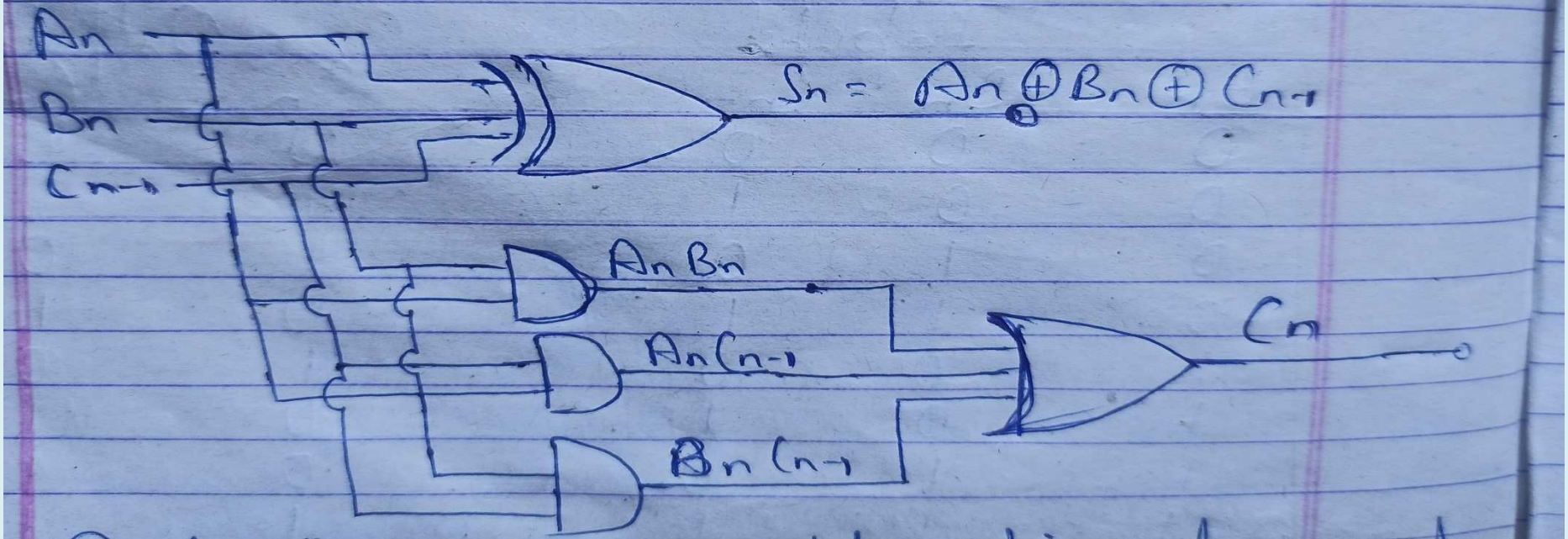
$S_n = \bar{A}_n \bar{B}_n C_{n-1} + \bar{A}_n B_n \bar{C}_{n-1} + A_n \bar{B}_n \bar{C}_{n-1} + A_n B_n C_{n-1}$

$S_n = \bar{A}_n (B_n \oplus C_{n-1}) + A_n (B_n \odot C_{n-1}) = A_n \oplus B_n \oplus C_{n-1}$

Expression for C_n is given as :-

$C_n = B_n C_{n-1} + A_n C_{n-1} + A_n B_n$



Realization of Full Adder Using logic gates.

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Refer book- Modern Digital Electronics by RP Jain.

Thank You