TOPIC :- Voltage-Controlled Oscillator (VCO)

The voltage Controlled oscillator (VCO) is an standard Sinusoidal oscillator ~~like~~ with the capacitors replaced by a varactor to provide a voltage-controlled frequency. It could be a 555 based circuit. In other words, the FM signals generator is also called VCO.

Fig.(1) shows a simplified schematic diagram of a VCO FM generator where a varactor diode is employed to convert the instantaneous value of the modulating signal to the change in frequency. A parallel resonant circuit containing the varactor diode (D) is used in the collector circuit of the transistor Q forming a tuned-collector oscillator.

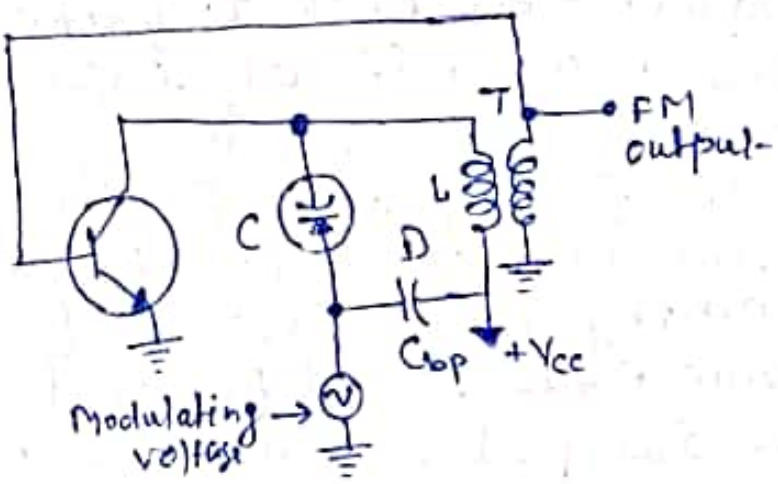


Fig (1)

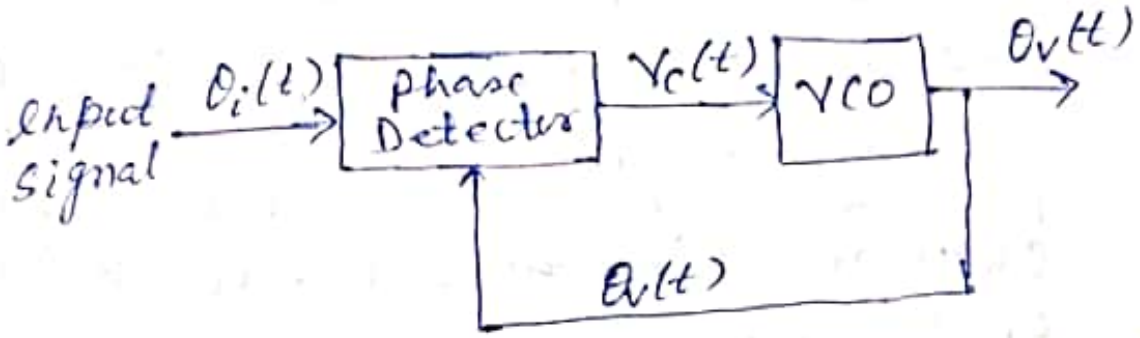
• Millman's Integrated electronics (Mc Graw Hill). JACOB MILLMAN, CHRISTOS.....

Phase Locked Loops (PLLs)

A PPL compares the phase of the input signal with the phase of an internally generated periodic signal and uses negative feedback to make these two phases nearly equal. If an input signal is suddenly applied to a PLL circuit, the circuit takes ~~place~~ a finite time to respond, at the end of which the phases of the incoming and internally generated signals become equal, independent of time, and then the PLL is said to be "locked."

Fig (2) shows the basic diagram of a first-order PLL. The "phase detector" produces an output voltage, $V_c(t)$, that is proportional to the difference in the phases of the input voltage and the VCO output $V_v(t)$. The output of the phase detector is fed to the voltage Controlled Oscillator (VCO). The frequency of the output

signal of the VCO is directly proportional to its input control voltage $V_c(t)$. Thus we can write the following general equation for the PLL.



Fig(2): Simple block diagram of a PLL

$$V_c(t) = K_D[\theta_i(t) - \theta_v(t)] \longrightarrow (1)$$

and $\omega_v(t) = \omega_{FR} + K_o V_c(t)$ $\longrightarrow (2)$

where θ_i and θ_v are the total phase of the input and VCO signals respectively; K_D is the gain of the phase detector; ω_v is the frequency of the VCO output. ω_{FR} is the "free-running" frequency and K_o is the voltage-to-frequency conversion factor of the VCO.

Operation:- To understand the operation of the PLL, let us consider the following cases and the total phase $\theta(t)$ is assumed that-

$$\theta(t) = \omega t + \phi(t)$$

Case 1:- when $\omega_i = \omega_{FR}$, $\phi_i = \phi_v = 0$.
If the input frequency and phase are equal to the VCO free-running frequency and phase, respectively, then the phase detector output will be zero and the PLL will be in its locked state. No changes will be occur as a function of time.

Case 2: $\omega_i = \omega_{FR}$, $\phi_i = 0$, $\phi_v \neq 0$

At $t=0$, $V_c(t) = K_D[\theta_i(t) - \theta_v(t)]$

$= K_D[\phi_i - \phi_v]$

If $\phi_v > 0$ at $t=0$, then $V_c(t=0)$ will be non-zero and negative. Hence from Eq (2), the VCO frequency will be smaller than ω_{FR}. This will cause the phase ϕ_v to vary. Hence $V_c(t) = K_D(\theta_i - \theta_v)$ will vary continuously with time, which will make the VCO frequency vary continuously with time. This will continue until the negative feedback causes the frequency of the VCO to become ω_{FR} and its phase to become zero. At this point, the loop will become locked.

Mathematically, we can write

$\theta_i(t) = \omega_{FR} t$ and

$\theta_v(t) = \omega_v t + \phi_v$

where ϕ_v is the initial phase difference between the input and VCO signals, and is not a function of time.
then from Eq^{n} (1) and (2),

$V_c(t) = K_D[\omega_{FR} t - \omega_v(t) \cdot t - \phi_v]$

$= K_D[\omega_{FR} t - \omega_{FR}(t) \cdot t - K_0 V_c(t) \cdot t - \phi_v]$

Therefore

$$V_c(t) = \frac{-K_D \phi_v}{1 + K_D K_0 t} \longrightarrow (3)$$

The above equation tells us that at $t=0$, $V_c = -K_0 \phi_v$, and as t tends to infinity, $V_c(t)$ tends to 0, hyperbolically, which conforms our qualitative description.

Case 3: $\omega_i > \omega_{FR}$, $\phi_i = \phi_v = 0$.
In this case, there will be a non-zero control voltage (V_c) at the input of the VCO, at $t=0$. The VCO frequency will adjust itself through the feedback loop and in the locked steady-state condition, it will become equal to ω_i. For a VCO frequency not equal to ω_{FR}, a non-zero control voltage must exist at its input; and for the phase detector

output to be non-zero, a steady-state phase difference between input and VCO signals must exist. In the locked state, therefore, the frequencies of the input and VCO signals will be equal, but a small phase difference will exist between them.

From eqn (1) and (2), we have

$$V_c(t) = K_D[\omega_i \cdot t - \omega_v(t) \cdot t]$$

$$= K_D[\omega_i \cdot t - \omega_{FR}(t) \cdot t - K_o V_c(t) \cdot t]$$

Therefore,

$$V_c(t) = \frac{K_D(\omega_i - \omega_{FR})t}{1 + K_D K_o t}$$

Then from equation (2), we have

$$\omega_v(t) = \frac{\omega_{FR} + K_o K_D \omega_i t}{1 + K_D K_o t} \longrightarrow (4)$$

From these two equations, we find that, at $t=0$, $V_c(t)=0$ and $\omega_v = \omega_{FR}$. This is as expected, because at $t=0$, with $\phi_i = \phi_v = 0$, $V_c(t) = K_D[\omega_i t - \omega_{FR} \cdot t] = 0$, and hence the VCO frequency is ω_{FR}. As t tends to infinity,

$$V_c(t) = \frac{(\omega_i - \omega_{FR})}{K_o} \text{ and } \omega_v = \omega_i$$

Thus the VCO frequency becomes equal to the input frequency (hence locking the PLL) and V_c attains a steady-state value proportional to the difference between the input signal frequency and the VCO free-running frequency. The phase difference $(\theta_i - \theta_v)$ in the locked state will be

$$\theta_i - \theta_v = \phi_i - \phi_v = \frac{V_c}{K_D} = \frac{(\omega_i - \omega_{FR})}{K_D K_o} \longrightarrow (5)$$

These equation show that in the locked state, a small difference will exist between input and output phase, but the frequencies will be exactly equal, which is one of the reason for the wide utility of the PLL.

Application:- phase locked loops, have become an integral part of many different communi-cation systems, and many digital systems, ever since the advent of integrated circuits. Some major application of PLLs are in frequency and phase demodulation, frequency synthesis, clock generation and recovery, reduction of jitter in circuits, etc.