Topic:- IC-555 TIMER

P.G - III Sem

The IC timer 555 is one of the most versatile linear integrated circuit to produce accurate and highly stable time delays on oscillation or to produce timing interval. The timer can operate in any of the two modes, i.e as a monosta multivibrator or as an astable multivib

The 555-timer can be considere a functional block that contains tw comparator, two transistors, three equ resistors, a flip-flop and an output sta The block diagram of the 555-timer shown in fig (1)

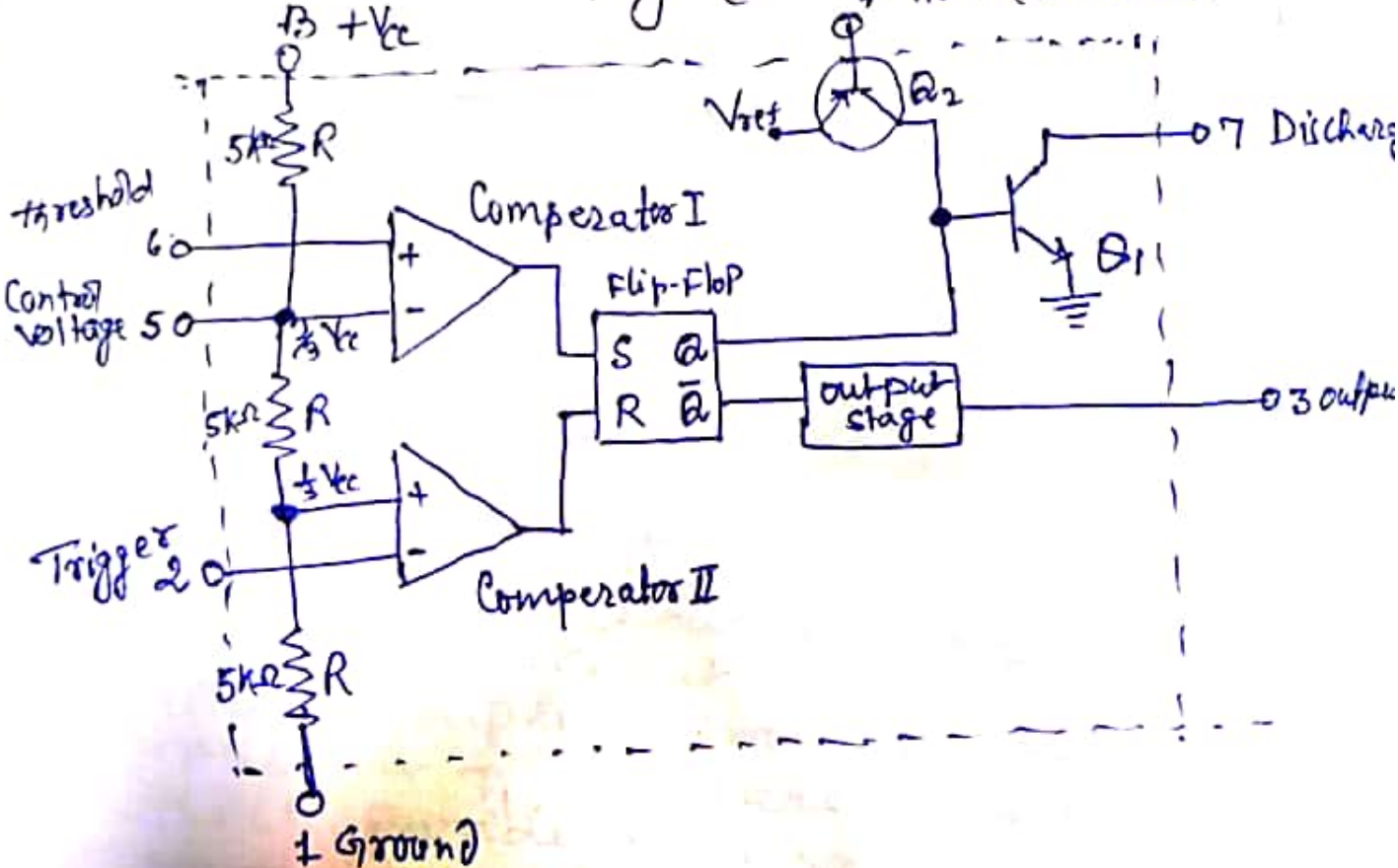


Fig (1)

pin 1: (Ground):→ It is the chip ground and all voltages are measured with respect to this terminal.

pin 2: (Trigger):— The output of the timer can be controlled by this pin. The output is low if the voltage at this pin is greater than 2/3 Vcc. In case a negative-going pulse of amplitude larger than 1/3 Vcc is applied to this pin, the comparator II output goes low, which in turn flip flop makes the output high. The output will remain high as long as the trigger terminal has a low voltage.

pin 3: (Output): The complementary signal out of the flip-flop goes through an output stage and becomes the output of the timer.

pin 4: (Reset): In most of the applications pin4 is not used and this pin is connected to supply voltage, +Vcc in order to avoid any false triggering.

pin 5: (Control voltage): The pulse width of the output waveform can be varied by imposing a voltage at this pin.

pin 6: (Threshold) when the voltage at this pin is greater than or equal to $\frac{2}{3}$ Vcc, the output of the comparator I goes high which makes the output of the timer low.

pin 7: (Discharge): A capacitor is connected externally to ground at this pin. Internally the collector of the discharge transistor is coming at this pin. Now a high O/P from the flip-flop makes the transistor off i.e open circuit and external

Capacitor charges at a rate determined by external RC network. When the output ③ is low, transistor gets saturated and external capacitor discharges.

Pin 8: (Supply + V_{cc}). The 555-timer works with supply voltage +5 volts to +18 volts with respect to ground (pin 1).

Fig (2) shows the pin-diagram of 8-pin DIP 555-timer.

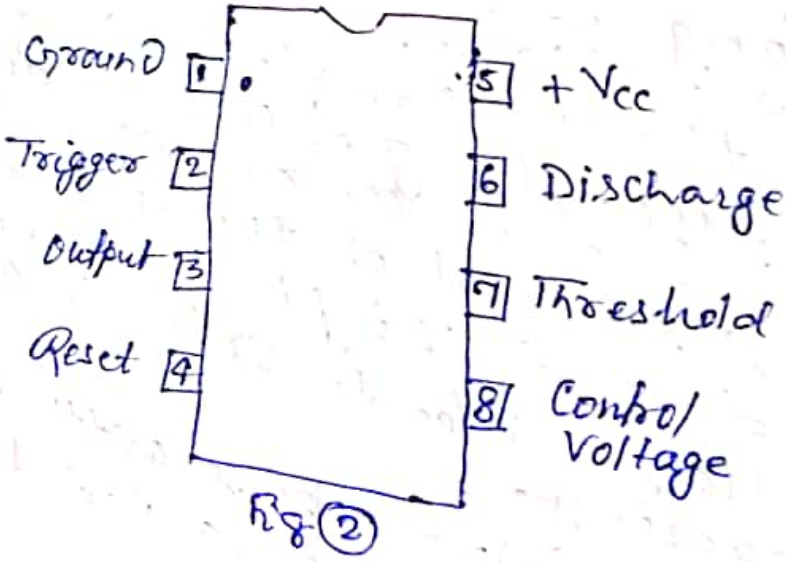


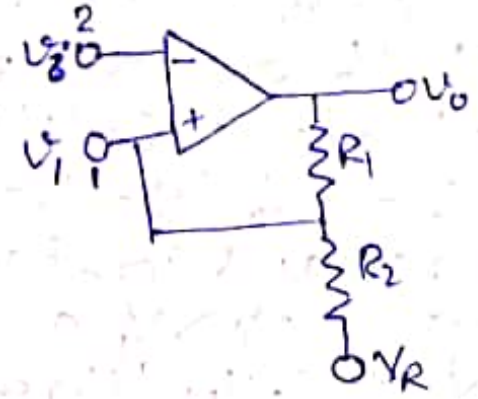
Fig ②

(b)

SCHMITT TRIGGER

Schmitt trigger is a sensitive to changes in the level of the input voltage V_i and is used to convert a slowly changing input waveform into a 'squared' output with very fast rise and fall times.

It is stable in one state and when triggered by a slowly varying input, it makes a very fast transition to the alternate state. Further when input returns to its original value, the circuit returns to its stable state making a very fast transition. The width of the output pulse is therefore determined by the shape and width of the input waveform.



Fig(1): Schmitt Trigger

By using positive feedback, the gain may be increased greatly, e.g., if loop gain $-\beta A_V$ be adjusted to unity, then gain with feedback A_{Vf} becomes ∞.

Large gain implies that for a small change in input, output changes greatly and the circuit thus becomes sensetive to the level of input voltage. ~~the threshold voltage for~~ If loop gain $-\beta A_V > 1$ then output waveform is virtually discontinuous at the comparison voltage. The threshold voltages for $v_i < V_1$ and $v_i > V_1$ for the circuit are different and the difference of two is accounted as hysteresis or backlash.

Assume that $v_i < V_1$ and $v_o = +V_0$ then as shown in fig (1)

$$v_1 = \left(\frac{R_1}{R_1+R_2}\right)V_R + \left(\frac{R_2}{R_1+R_2}\right)V_0 = V_1 \text{ (say)}$$

Now, if we increase input voltage, v_i then until $v_i = V_1$, output v_o remains constant at V_0 but when v_i exceeds V_1, the output atonce switches regeneratively to $v_o = -V_0$ (the transition is abrupt) and remains constant at this value as long as $v_i > V_1$ as shown in fig (2a). $v_i = V_1$ is called "threshold or triggering voltage"

for $v_i > V_1$, value of v_1 is

$$v_1 = \left(\frac{R_1}{R_1+R_2}\right)V_R - \left(\frac{R_2}{R_1+R_2}\right)V_0 = V_2 \text{ (say)}$$

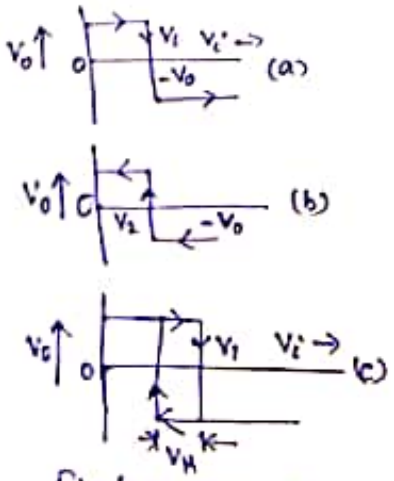
If we now decrease input voltage, then until $v_i = V_2$, output v_o remains at $-V_0$. At $v_i = V_2$, output abruptly switches to $+V_0$.

Thus

→ at $v_i = V_1$, when input voltage, v_i is increasing, output voltage switches to $-V_0$.

→ at $v_i = V_2$ when input voltage, v_i is decreasing output voltage v_o switches to $+V_0$

This switching is abrupt and we get a "squared" output as shown in fig (3)



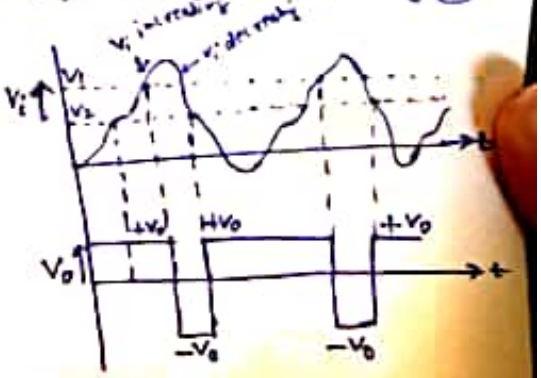


Fig (3)
'Squared' output for slowly varying input

Fig (2): Transfer characteristics
(a) increasing v_i (b) decreasing v_i
(c) composite input/output curve.

Thus we observe that circuit triggers abruptly as shown in transfer characteristics of fig 2 (a), (b), (c). We also note that as $V_1 > V_2$, circuit triggers at a higher voltage for increasing than for decreasing input on account of hysteresis