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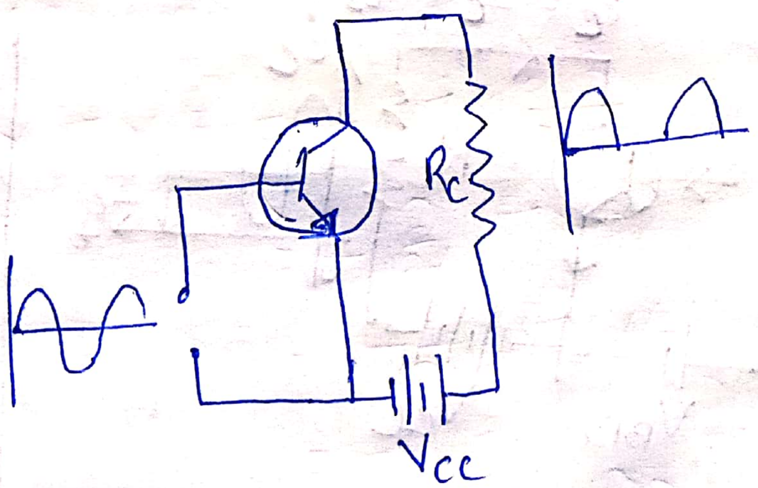
Topic: TRANSISTOR BIASING

U.G - III

Consider an npn transistor circuit shown in fig(1a). During the positive half-cycle of the signal, base is +ve w.r.t emitter and hence base emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is revers-biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is ~~un~~ "unfaithful amplification"



Fig(1a)

Now, a battery source V_{BB} in the base circuit is introduced as shown in fig(1b). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as "zero signal collector current" (I_C). During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows that for faithful amplification, proper zero signal collector current must flow.

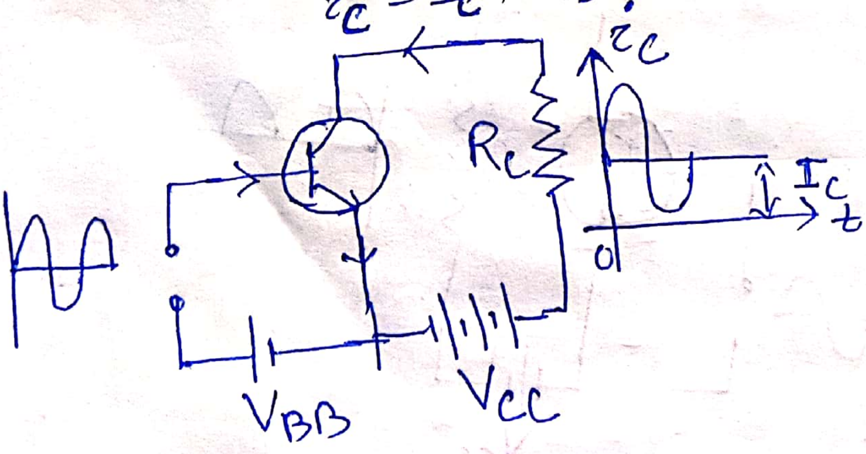


Fig. (1b)

Total i_C = Collecter current

I_C = Zero signal current

i_{cs} = Current due to signal.

Thus transistor biasing is the process of flow of zero signal collector current and the maintence of proper collector-emitter voltage during the passage of signal. The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of the signal.

The following are the most commonly used methods of obtaing transistor biasing from one source of supply V_{CC}

(i) Base resistor method
(ii) Emitter bias method
(iii) Biasing with collector-feedback resistor
(iv) voltage-divider bias

(i) Base Resistor Method

In this method, a high resistance R_B of several hundred kΩ is connected between the base and +ve end of supply for npn transistor as shown in fig (2) and between base and -ve end of supply for pnp transister. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B because base is +ve w.r.t emitter i.e base-emitter junction is forward biased. The required value of zero signal base current I_B and hence $I_C = \beta I_B$ can be made to flow by selecting the proper value of base resistor R_B.

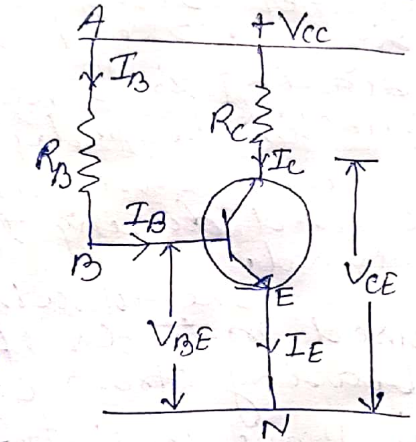


Fig (2)

Circuit Analysis:-

We have to find the value of R_B so that required collector current flows in the zero signal condition. Let I_C be the required zero signal collector current.

$$\therefore I_B = \frac{I_C}{\beta}$$

Considering the closed circuit ABENA and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\text{or, } I_B R_B = V_{CC} - V_{BE}$$

$$\therefore R_B = \frac{V_{CC} - V_{BE}}{I_B} \longrightarrow (1)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from eqn (1).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from eqn (1) that

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence R_B can always be found directly and for this ~~region~~ reason, this method is sometimes called <u>fixed bias method</u>.

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